# LENDI INSTITUTE OF ENGINEERING AND TECHNOLOGY

An Autonomous Institution
Approved by AICTE & Permanently Affiliated to JNTUK, Kakinada
Accredited by NAAC with "A" Grade and NBA (CSE, EEE & ME)
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## DEPARTMENT OF ELECTRONICS AND COMMUNICATIONENGINEERING

**M.Tech (Embedded Systems & VLSI Design) Course Structure –R22**

(w.e.f the academic year 2022-23)

### I Year -I Semester

| S.No | Course Code | Subject Name | L | P | Credits |
|---|---|---|---|---|---|
| 1 | EC-ESVD1101 | RTL Simulation and Synthesis with PLDs | 3 | 0 | 3 |
| 2 | EC-ESVD1102 | Microcontrollers and Programmable Digital Signal Processors | 3 | 0 | 3 |
| 3 | EC-ESVD1103 | **Program Elective-I** | 3 | 0 | 3 |
| | EC-ESVD1103.1 | 1. Digital Signal and ImageProcessing | | | |
| | EC-ESVD1103.2 | 2. ParallelProcessing | | | |
| | EC-ESVD1103.3 | 3. VLSI signalprocessing | | | |
| 4 | EC-ESVD1104 | **Program Elective -II** | 3 | 0 | 3 |
| | EC-ESVD1104.1 | 1. Programming Languages for EmbeddedSystems | | | |
| | EC-ESVD1104.2 | 2. System Design with EmbeddedLinux | | | |
| | EC-ESVD1104.3 | 3. CAD of DigitalSystem | | | |
| 5 | EC-ESVD1105 | **Program Elective-III** | 3 | 0 | 3 |
| | EC-ESVD1105.1 | 1. IOT and itsApplications | | | |
| | EC-ESVD1105.2 | 2. Hardware Software co-design | | | |
| | EC-ESVD1105.3 | 3. Artificial Intelligence | | | |
| 6 | EC-ESVD1106 | Research Methodology and IPR | 2 | 0 | 2 |
| 7 | EC-ESVD1107 | RTL Simulation and Synthesis with PLDs Lab | 0 | 4 | 2 |
| 8 | EC-ESVD1108 | Microcontrollers and Programmable Digital Signal Processors Lab | 0 | 4 | 2 |
| | | **Total** | **17** | **8** | **21** |

### I Year –IISemester

| S.No | Course Code | SubjectName | L | P | Credits |
|---|---|---|---|---|---|
| 1 | EC-ESVD1201 | Analog and Digital CMOS VLSI Design | 3 | 0 | 3 |
| 2 | EC-ESVD1202 | Real Time Operating Systems | 3 | 0 | 3 |
| 3 | EC-ESVD1203 | **Program Elective-IV** | 3 | 0 | 3 |
| | EC-ESVD1203.1 | 1. MemoryArchitectures | | | |
| | EC-ESVD1203.2 | 2. SoCDesign | | | |
| | EC-ESVD1203.3 | 3. Low power VLSIDesign | | | |
| 4 | EC-ESVD1204 | **Program Elective -V** | 3 | 0 | 3 |
| | EC-ESVD1204.1 | 1. Communication Buses andInterfaces | | | |
| | EC-ESVD1204.2 | 2. Network Security andCryptography | | | |
| | EC-ESVD1204.3 | 3. Physical designautomation | | | |
| 5 | EC-ESVD1205 | **Open Elective -I** | 3 | 0 | 3 |
| | EC-ESVD1205.1 | BusinessAnalytics | | | |
| | EC-ESVD1205.2 | IndustrialSafety | | | |
| | EC-ESVD1205.3 | OperationsResearch | | | |

| | | | | | |
|---|---|---|---|---|---|
| | EC-ESVD1205.4 | Cost Management ofEngineering Projects | | | |
| | EC-ESVD1205.5 | CompositeMaterials | | | |
| | EC-ESVD1205.6 | Waste toEnergy | | | |
| 6 | EC-ESVD1206 | Analog and Digital CMOS VLSI Design Lab | 0 | 4 | 2 |
| 7 | EC-ESVD1207 | Real Time Operating Systems Lab | 0 | 4 | 2 |
| 8 | EC-ESVD1208 | **Mini Project** | 0 | 4 | 2 |
| | | **Total** | **15** | **8** | **21** |

*Students be encouraged to go to Industrial Training/Internship for at least 2-3 weeks during semester break.

**II Year – ISemester**

| S.No | Course Code | Subject Name | L | P | Credits |
|---|---|---|---|---|---|
| 1 | AC-ERPW1101 | **Audit Course 1** | 2 | 0 | 0 |
| 2 | AC-RMIP1201 | **Audit Course 2** | 2 | 0 | 0 |
| 3 | EC-ESVD2103 | Dissertation Phase -I /Industrial Project **(to be continued and evaluated next semester)** | 0 | 20 | 10 |
| | | **Total** | **4** | **20** | **10#** |

#Evaluated and Displayed in IV Semester Marks list.

**Audit Course 1& 2**

1. English for Research PaperWriting
2. DisasterManagement
3. Sanskrit for Technical Knowledge
4. ValueEducation
5. Constitution ofIndia
6. PedagogyStudies
7. Stress Management byYoga
8. Personality Development through Life EnlightenmentSkills.

**II Year – II Semester**

| S.No | Course Code | Subject Name | L | P | Credits |
|---|---|---|---|---|---|
| 1 | EC-ESVD2201 | Project/ Dissertation Phase-II **(continued from III semester)** | 0 | 32 | 16 |
| | | **Total** | **0** | **32** | **16** |

| Subject Code | Subject Name | Hours | Credits |
|---|---|---|---|
| EC-ESVD1101 | RTL Simulation and Synthesis with PLDs | 3 | 3 |

**Course Objectives:**

Faculty is going to

- Introduce Verilog HDL for the design and functionality verification of a digitalcircuit.
- Understand the design of data path and control circuits for sequentialmachines.
- Illustrate the steps in design and development of digital Circuit Design.
- Summarize the static timing analysis of digital design.
- Introduce the concept of realizing a digital circuit usingPLDs

**Course Outcomes:**

After completion of course, students are able to

1. Develop digital circuits using Verilog HDL programming.
2. Utilize State Charts and Finite State Machine for the design of different sequential circuits.
3. Summarize the steps for design and verification of digital circuits.
4. Interpret the static timing analysis of different digital circuits.
5. Verify the functionality of the digital designs usingPLDs.

**UNIT-I:**

**Verilog HDL:** Importance of HDLs, Lexical Conventions of VerilogHDLGate level modeling: Built in primitive gates, switches, gate delays Data flow modeling: Continuous and implicit continuous assignment, delays Behavioral modeling: Procedural constructs, Control and repetition Statements, delays, function and tasks.

**Learning Outcomes:**

1. Summarize different structures of Verilog HDL programming. **(L2)**
2. Construct various digital circuits using Verilog HDL programs.**(L3)**

**UNIT-II:**

**Digital Design:** Design of BCD Adder, State graphs for control circuits, shift and add multiplier, Binary divider.FSM and SM Charts: Finite state diagram, Implementation of sequence detector using FSM, State machine charts, Derivation of SM Charts, Realization of SM Chart, Implementation of Binary Multiplier.

**Learning Outcomes:**

1. Outline the importance of state machine and fine state machine in design of sequential circuits.**(L2)**
2. Make use of Finite State Machine to design various digital sequential circuits.**(L3)**

**UNIT-III:**

**ASIC Design Flow:** Simulation, simulation types, Synthesis, synthesis methodologies, translation, mapping, optimization, Floor planning, Placement, routing, Clock tree synthesis, Physical verification.

**Learning Outcomes:**

1. Summarize the various simulation and synthesis methods in functional verification of digital circuits.**(L2)**
2. Outline the various optimization and verification methods used in design of digital circuits.**(L2)**

**UNIT-IV:**

**Static Timing Analysis:** Timing paths, Meta-stability, Clock issues, Need and design strategies for multi-clock domain designs, setup and hold time Violations, steps to remove Setup and hold time violations.

**Learning Outcomes:**

1. Summarize the challenges and issues in employing clock based digital circuit design. **(L2)**
2. Illustrate the static timing analysis of digital circuits with various clock-based optimization techniques.**(L3)**

**UNIT-V:**

**DigitalDesignusingPLD's:**ROM,PLA,PAL-RegisteredPAL's,ConfigurablePAL's,GAL.CPLDs: Features, programming and applications using complex programmable logic devices. FPGAs: Field Programmable gate arrays Logic blocks, routing architecture, designflow.

**Learning Outcomes:**

1. Interpret the design of digital circuits with PLD's. **(L2)**
2. Extend the digital design with the implementation of digital circuits in FPGAs.**(L2)**

**TEXT BOOKS:**


1. Verilog HDL, A Guide to Digital Design and Synthesis Samir Palnitkar, 2nd Edition,2003
2. Fundamentals of Logic Design, Charles H. Roth, 5th Edition. Cengage Learning,2010.
3. Verilog HDL Synthesis a Practical Primer by Bhasker J, 1st edition,1998
4. Modern Digital Electronics P Jain, 3rd Edition, TMH,2003.


**REFERENCES:**


1. Donald D Givone, "Digital principles and Design", TMH,2016
2. Data Sheets for CPLD & FPGA architectures,1996.
3. Bob Zeidman, "Designing with FPGAs & CPLDs", CMP Books,2002.
4. Richard S. Sandige, "Modern Digital Design", MGH, International Editions, 1990


**COURSE OUTCOMES VS POs MAPPING (**DETAILED; HIGH:3; MEDIUM:2; LOW:1**):**

| SNO | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 | PSO1 | PSO2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO.1** | 3 | 2 | 2 | - | 2 | - | - | - | - | 2 | - | 2 | 2 | 1 |
| **CO.2** | 3 | 2 | 2 | 2 | 2 | - | - | - | - | 2 | - | 2 | 2 | 1 |
| **CO.3** | 3 | 2 | 2 | 2 | 2 | - | - | - | - | 2 | - | 2 | 2 | 1 |
| **CO.4** | 3 | 2 | 2 | 2 | 2 | - | - | - | - | 2 | - | 2 | 2 | 1 |
| **CO.5** | 3 | 2 | 2 | 2 | 2 | - | - | - | - | 2 | - | 2 | 2 | 1 |
| **CO*** | 3 | 2 | 2 | 2 | 2 | - | - | - | - | 2 | - | 2 | 2 | 1 |

***5. * For Entire Course, PO & PSO Mapping***

| Subject Code | Subject Name | Hours | Credits |
|---|---|---|---|
| EC-ESVD1102 | Microcontrollers and Programmable Digital SignalProcessors | 3 | 3 |

**CourseObjectives:**

Faculty is going to

- Understand the ARM cortex M3 processor design.
- Show the importance of interrupts and their function in the cortex processors.
- Understand the working controller LPC17xx with additional features.
- Show the design of programmable DSP processors and their features.
- Understand the working of a C6000 family-based programming.

**Course Outcomes:**

At the end of this course, students will be able to

1. Outline the features and functional units of a ARM cortex processor.
2. Interpret the working of ARM cortex interrupts for its program design.
3. Summarize the features of LPC17xx microcontrollers as an embedded controller.
4. Explain the fundamental units that compose the design of programmable DSP processors.
5. Extend the design of DSP processors to TI's C6000 family towards application development.

**UNIT-I**

**ARM Cortex-M3 processor:** Applications, Programming model – Registers, Operation modes, Exceptions and Interrupts, Reset Sequence Instruction Set, Unified Assembler Language, Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations, Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces

**Learning Outcomes:**

1. List the working design of a ARM cortex M3 processor. **(L2)**
2. Summarize the architecture design and features as part of a typical RISC machine like ARM.**(L3)**

**Unit-II**

Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behavior, Fault Exceptions, Supervisor and dependable Service Call, Nested Vectored Interrupt Controller, Basic Configuration.

**Learning Outcomes:**

1. Understand the implementation of interrupts in a ARM based processor.**(L2)**
2. Understand the interrupt based system design in ARM processorss.**(L3)**

**Unit-III**

**LPC 17xx microcontroller**- Internal memory, GPIOs, Timers, ADC, UART and other serial interfaces, PWM, RTC, WDT.

**Learning Outcomes:**

1. Review the various features of a LPC17XX microcontroller. **(L2)**
2. Recognize the importance of features like GPIOs, Timers, ADC etc.**(L2)**

**Unit-IV**

**Programmable DSP (P-DSP) Processors:** Harvard architecture, Multi port memory, architectural structure of P-DSP- MAC unit, Barrel shifters, Introduction to TI DSP processor family.

**Learning Outcomes:**

1. Describe the architecture features of a typical programmable DSP processors. **(L2)**
2. Identify the importance of barrel shifter within the DSP processors.**(L2)**

**Unit-V**

VLIW architecture and TMS320C6000 series, architecture study, data paths, cross paths, Introduction to Instruction level architecture of C6000 family, Assembly Instructions memory addressing, for arithmetic, logical operations. Code Composer Studio for application development for digital signal processing

**Learning Outcomes:**

1. Explain the VLIW and typical features in a TMS320C6000 family DSP. **(L2)**
2. Summarize the instructions and the development of applications for DSP processor.**(L2)**

**TEXT BOOKS:**


1. Joseph Yiu, "The definitive guide to ARM Cortex-M3", Elsevier, 2ndEdition
2. Venkatramani B. and Bhaskar M. "Digital Signal Processors: Architecture,Programming and Applications", TMH , 2ndEdition
3. Sloss Andrew N, Symes Dominic, Wright Chris, "ARM System Developer'sGuide: Designing and Optimizing", Morgan KaufmanPublication


**REFERENCE BOOKS:**


2. Steve furber, "ARM System-on-Chip Architecture", PearsonEducation
3. Frank Vahid and Tony Givargis, "Embedded System Design",Wiley
4. Technical references and user manuals onwww.arm.com.


**COURSE OUTCOMES VS POs MAPPING (**DETAILED; HIGH:3; MEDIUM:2; LOW:1**):**

| SNO | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 | PSO1 | PSO2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO.1** | 3 | 2 | 2 | 2 | 2 | - | - | - | - | 2 | - | 2 | 2 | - |
| **CO.2** | 3 | 2 | 2 | 2 | 2 | - | - | - | - | 2 | - | 2 | 2 | - |
| **CO.3** | 3 | 2 | 2 | 2 | 2 | - | - | - | - | 2 | - | 2 | 2 | - |
| **CO.4** | 3 | 2 | 2 | 2 | 2 | - | - | - | - | 2 | - | 2 | 2 | - |
| **CO.5** | 3 | 2 | 2 | 2 | 2 | - | - | - | - | 2 | - | 2 | 2 | - |
| **CO*** | 3 | 2 | 2 | 2 | 2 | - | - | - | - | 2 | - | 2 | 2 | - |

***1. * For Entire Course, PO & PSO Mapping***

| Subject Code | Subject Name | Hours | Credits |
|---|---|---|---|
| EC-ESVD1103.1 | Digital Signal and ImageProcessing | 3 | 3 |

**Program Elective-I**

**Course Objectives:**

Faculty is going to

- Introduce the discrete time signal analysis in various domains.
- Develop digital filters for digital signal enhancement.
- Provide the analysis of finite word length effect on digital value of a signal.
- Consider image processing with enhancement and restoration methods.
- List the methods of image compression and color processing.

**Course Outcomes:**

At the end of this course, students will be able to

1. Analyze discrete-time signals and systems in various domains ( i.e Time, Z andFourier). (L4)
2. Design the digital filters (both IIR and FIR) from the givenspecifications. (L3)
3. Analyze the quantization effects in digital filters and understand the basics of imagesampling, quantization and imagetransforms. (L4)
4. Understand the concepts of image enhancement, image restoration and imagesegmentation. (L2)
5. Summarize the various methods involved in image compression and fundamentals in color image processing. (L2)

**UNIT -I**

Review of Discrete Time signals and systems, Characterization in time, Z and Fourier domain, Fast Fourier Transform using Decimation in Time (DIT) and Decimation In Frequency (DIF) Algorithms.

**Learning Outcomes:**

1. Utilize the transform domains of Z and Fourier domain for signal and system analysis. (L3)
2. Determine the necessity and application using DIT and DIF based signal processing. (L3)

**UNIT-II**

**IIR Digital Filters:** Introduction, Analog filter approximations – Butter worth and Chebyshev, Design of IIR Digital filters from analog filters using Impulse Invariance, Bilinear Transformation methods.

**FIR Digital Filters:** Introduction, Design of FIR Digital Filters using Window Techniques, Frequency Sampling technique, Comparison of IIR & FIR filters.

**Learning Outcomes:**

1. Utilize the various IIR digital filters for signal detection and correction. (L3)
2. Utilize the various FIR digital filters for signal detection and correction. (L3)

**UNIT-III**

**Analysis Of Finite Word length Effects:** The Quantization Process and Errors, Quantization of Fixed-Point Numbers, Quantization of Floating-Point Numbers, Analysis of Coefficient Quantization effects.

**Introduction To Digital Image Processing:** Introduction, components in image processing system, Applications of Digital image processing, Image sensing and acquisition, Image sampling, Quantization, Basic Relationships between pixels, Image Transforms: 2D-DFT, DCT, Haar Transform.

**Learning Outcomes:**

1. Identify the effects of quantization on fixed- and floating-point number formats. (L2)
2. Introduce the basics of digital image processing. (L2)

**UNIT-IV**

**Image Enhancement:** Intensity transformation functions, histogram processing, fundamentals of spatial filtering, smoothing spatial filters, sharpening spatial filters, the basics of filtering in the frequency domain, image smoothing using frequency domain filters, Image Sharpening using frequency domain filters, Selective filtering.

**Image Restoration:** Introduction, restoration in the presence of noise only-Spatial Filtering, Periodic Noise Reduction by frequency domain filtering, Linear, Position –Invariant Degradations, Estimating the degradation function, Inverse filtering, Minimum mean square error (Wiener) filtering.

**Image Segmentation:** Fundamentals, point, line, edge detection, thresholding, region based segmentation.

**Learning Outcomes:**

1. Discuss the implementation of filters, transformation functions and histogram processing for image enhancement. (L3)
2. Implementation of filters to reduce noise and improve image quality and restoration. (L3)
3. Determine the fundamental steps for segmenting the images. (L2)

**UNIT-V**

**Image Compression:** Fundamentals, Basic compression methods: Huffman coding, Arithmetic coding, Run-Length coding, Block Transform coding, Predictive coding, Wavelet coding.

**Color Image Processing:** color fundamentals, color models, pseudo color image processing, basics of full color image processing, color transformations, smoothing and sharpening. Image segmentation based on color, noise in color images, color image compression.

**Learning Outcomes:**

1. Review the basic compression methods of images. (L2)
2. Implement the transformation and fundamentals of color image processing. (L3)

**TextBooks:**


1. Digital Signal Processing, Principles, Algorithms, and Applications: John G. Proakis, Dimitris G.Manolakis,PearsonEducation/PHI,2007.
2. S. K. Mitra. "Digital Signal Processing – A Computer based Approach", TMH, 3rdEdition,2006
3. Rafael C.Gonzalez and Richard E. Woods, "Digital Image Processing", Pearson Education,2011.
4. S.Jayaraman, S.Esakkirajan, T.Veerakumar, "Digital Image Processing", Mc Graw Hill Publishers, 2009


**Reference Books**


1. Digital Signal Processing: Andreas Antoniou, TATA McGraw Hill ,2006
2. DigitalSignalProcessing:MHHayes,Schaum"sOutlines,TATAMc-GrawHill,2007.
3. Anil K. Jain, "Fundamentals of Digital Image Processing," Prentice Hall of India,2012.


**COURSE OUTCOMES VS POs MAPPING (**DETAILED; HIGH:3; MEDIUM:2; LOW:1**):**

| SNO | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 | PSO1 | PSO2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO.1** | 3 | 1 | 1 | - | 2 | - | - | - | - | 2 | - | 2 | 2 | 1 |
| **CO.2** | 3 | 3 | 3 | 1 | 2 | - | - | - | - | 2 | - | 2 | 2 | 1 |
| **CO.3** | 3 | 3 | 3 | 1 | 2 | - | - | - | - | 2 | - | 2 | 2 | 1 |
| **CO.4** | 3 | 3 | 3 | 1 | 2 | - | - | - | - | 2 | - | 2 | 2 | 1 |
| **CO.5** | 3 | 3 | 3 | 1 | 2 | - | - | - | - | 2 | - | 2 | 2 | 1 |
| **CO*** | 3 | 3 | 3 | 1 | 2 | - | - | - | - | 2 | - | 2 | 2 | 1 |

**** For Entire Course, PO & PSO Mapping***

| Subject Code | Subject Name | Hours | Credits |
|---|---|---|---|
| EC-ESVD1103.2 | Parallel Processing | 3 | 3 |

**Program Elective-I**

**Course Objectives:**

Faculty is going to

- Introduce the features for parallel processing.
- Provide working of pipelining at different steps of computer.
- Discuss implementation of VLIW in different processors along with vector and multiprocessor architecture.
- Importance of multithreaded architecture and implementation.
- Introduce programming techniques for various parallel processing systems.

**Course Outcomes:**

At the end of this course, students will be able to

1. Identify various features necessary for design of a parallel processing systems. (L2)
2. Demonstrate the working and implementation of pipelining concept at various stages of computing. (L3)
3. Summarize the implementation of VLIW architecture in various modern processors. (L2)
4. Illustrate the implementation of multithreading for computer performance improvement. (L3)
5. Discover various programming techniques in development of various parallel processing systems. (L3)

**Unit-I:**Overview of Parallel Processing and Pipelining, Performance analysis, Scalability

**Learning Outcomes:**

1. List the features and basic architecture of parallel processing system. (L2)

**Unit-II:**Principles and implementation of Pipelining, Classification of pipelining processors, Advanced pipelining techniques, Software pipelining.

**Learning Outcomes:**

1. Understand the functioning of a pipeline concept for performance improvement. (L2)
2. Implementation of pipelining at various parts of a parallel computing system. (L3)

**Unit-III:** VLIW processors Case study: Superscalar Architecture- Pentium, Intel Itanium Processor, Ultra SPARC,MIPS on FPGA, Vector and Array Processor, FFT Multiprocessor Architecture

**Learning Outcomes:**

1. Understand the use of VLIW and its implementation in various Processors. (L2)
2. Discuss the concept of vector and array processor as a parallel processing scheme. (L2)

**Unit-IV:** Multithreaded Architecture, Multithreaded processors, Latency hiding techniques, Principles of multithreading, Issues and solutions

**Learning Outcomes:**

1. Understand the working of a multithreaded architecture. (L2)
2. Implementation of multithreaded architecture to overcome various challenges. (L3)

**Unit-V:**Parallel Programming Techniques: Message passing program development, Synchronous and asynchronous message passing, Shared Memory Programming, Data Parallel Programming, Parallel Software Issues. Operating systems for multiprocessors systems Customizing applications onparallel processingplatforms.

**Learning Outcomes:**

1. List various programming techniques useful for data parallel processing. (L2)

2. Design of operating systems for customization of applications on various parallel processing platforms. (L3)

**Text Books:**

1. Kai Hwang, Faye A. Briggs, "Computer Architecture and Parallel Processing", MGH InternationalEdition
2. Kai Hwang, "Advanced Computer Architecture",TMH
3. V. Rajaraman, L. Sivaram Murthy, "Parallel Computers",PHI.

**Reference Books:**

1. William Stallings, "Computer Organization and Architecture, Designing for performance "Prentice Hall, Sixthedition.
2. Kai Hwang, ZhiweiXu, "Scalable Parallel Computing",MGH.
3. David Harris and Sarah Harris, "Digital Design and Computer Architecture",Morgan.

**COURSE OUTCOMES VS POs MAPPING (**DETAILED; HIGH:3; MEDIUM:2; LOW:1**):**

| SNO | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 | PSO1 | PSO2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO.1** | 3 | 1 | - | - | - | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO.2** | 3 | 2 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO.3** | 3 | 3 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO.4** | 3 | 3 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO.5** | 3 | 3 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO*** | 3 | 3 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |

**** For Entire Course, PO & PSO Mapping***

| Subject Code | Subject Name | Hours | Credits |
|---|---|---|---|
| EC-ESVD1103.2 | VLSI Signal Processing | 3 | 3 |

**Program Elective-I**

**Course Objectives:**

Faculty is going to

- Introduce pipelining for design and development of DSP architecture for VLSI design.
- List various folding and unfolding architectures for multirate systems.
- Introduce the working of systolic architecture design.
- Show the working of various fast convolution methods.
- Design of lattice filter structure towards low power design.

**Course Outcomes:**

At the end of this course, students will be able to

1. Extend the existing or new DSP architectures towards suitable VLSI design. (L2)
2. Summarize the concepts of folding and unfolding algorithms andapplications. (L2)
3. Express the working of systolic architecture design. (L2)
4. Demonstrate the implementation of fast convolution algorithms for VLSI design. (L3)
5. Employ Low power design aspects of processors for signal processing and wirelessapplications. (L3)

**UNIT -I**

Introduction to DSP: Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms Pipelining and Parallel Processing.

Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power Retiming Introduction, Definitions and Properties, Solving System of Inequalities, Retiming Techniques.

**Learning Outcomes:**

1. Listing the DSP algorithms supporting VLSI design. (L2)
2. Demonstrate the use of pipeline and other methods to reduce the power requirements in a VLSI design. (L2)

**UNIT –II**

Folding and Unfolding: Folding- Introduction, Folding Transform, Register minimization Techniques, Register minimization in folded architectures, folding of Multirate systems, Unfolding- Introduction, An Algorithm for Unfolding, Properties of Unfolding, critical Path, Unfolding and Retiming, Applications of Unfolding.

**Learning Outcomes:**

1. Summarize the folding and unfolding architecture for various VLSI design improvement. (L2)

**UNIT -III**

Systolic Architecture Design: Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations contain Delays.

**Learning Outcomes:**

1. Understand the importance of systolic architecture design for VLSI in implementing signal processing. (L2)

**UNIT -IV**

Fast Convolution: Introduction – Cook-Toom Algorithm – Winogard algorithm – Iterated Convolution –

Cyclic Convolution – Design of Fast Convolution algorithm by Inspection

**Learning Outcomes:**

1. List various fast convolution methods for signal processing design. (L2)

**Unit V:** Digital lattice filter structures, bit level arithmetic, architecture, redundant arithmetic.Numerical strength reduction, synchronous, wave and asynchronous pipe lines, low power design.

Low Power Design: Scaling Vs Power Consumption, Power Analysis, Power Reduction techniques, Power Estimation Approaches

**Learning Outcomes:**

1. Introduce low power design structures for better vlsi design. (L2)

**Text Books:**


1. Keshab K. Parthi[A1], VLSI Digital signal processing systems, design and implementation[A2], Wiley, Inter Science,1999.
2. Mohammad Isamail and Terri Fiez, Analog VLSI signal and information processing, McGraw Hill, 1994
3. S.Y. Kung, H.J. White House, T. Kailath, VLSI and Modern Signal Processing, Prentice Hall, 1985.


**COURSE OUTCOMES VS POs MAPPING (**DETAILED; HIGH:3; MEDIUM:2; LOW:1**):**

| SNO | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 | PSO1 | PSO2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO.1** | 3 | 1 | - | - | - | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO.2** | 3 | 2 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO.3** | 3 | 3 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO.4** | 3 | 3 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO.5** | 3 | 3 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO*** | 3 | 3 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |

**** For Entire Course, PO & PSO Mapping***

| Subject Code | Subject Name | Hours | Credits |
|---|---|---|---|
| EC-ESVD1104.1 | Programming Languages for Embedded Systems | 3 | 3 |

**Program Elective -II**

**Course Objectives:**

Faculty is going to

- Introduce the concepts of embedded C and data structures for embedded design optimization.
- Importance of object-oriented programming for embedded system.
- Introduce CPP programming and its features for embedded programming.
- Show the importance of overloading and inheritance in embedded programming design.
- Use of templates and scripting language for program automation in embedded systems.

**Course Outcomes:**

At the end of this course, students will be able to

1. Discover the working of embedded 'C' and its implementation in a embedded system design. (L3)
2. Illustrate the importance of Object-Oriented Programming concepts for design of embedded systems. (L3)
3. Employ the CPP programming for use in a embedded system design. (L3)
4. Demonstrate the importance of overloading and inheritance for development of embedded programming. (L3)
5. Summarize the need of scripting languages with their implementation in embedded systems. (L3)

**Unit-I:** Embedded 'C' Programming Bitwise operations, Dynamic memory allocation, OS services. Linked stack and queue, Sparse matrices, Binary tree. Interrupt handling in C, Code optimization issues. Embedded Software Development Cycle and Methods (Waterfall, Agile)

**Learning Outcomes:**

1. Utilize the necessary changes of Embedded C programming. (L3)
2. Learn the optimization and embedded software development methods. (L2)

**Unit-II:**Object Oriented Programming Introduction to procedural, modular, object-oriented and generic programming techniques, Limitations of procedural programming, objects, classes, data members, methods, data encapsulation, data abstraction and information hiding, inheritance, polymorphism.

**Learning Outcomes:**

1. Summarize the different features of object oriented programming. (L2)
2. Demonstrate the working of classes, objects, data encapsulation, data abstraction. (L3)

**Unit-III:** CPP Programming: "cin","cout", formatting and I/O manipulators, new and deleteoperators,Definingaclass,datamembersandmethods,"this"pointer,constructors,destructors,friend function, dynamic memoryallocation.

**Learning Outcomes:**

1. Discuss different features of CPP programming. (L2)
2. Make use of CPP features like I/O manipulator, constructors and dynamic memory allocation for embedded firmware development. (L3)

**Unit-IV:** Overloading and Inheritance: Need of operator overloading, overloading the assignment, Overloading using friends, type conversions, single inheritance, base and derived classes, friend Classes, types of inheritance, hybrid inheritance, multiple inheritance, virtual base class, Polymorphism, virtual functions.

**Learning Outcomes:**

1. Explain the working of overloading and inheritance with in embedded firmware development. (L2)

**Unit-V:** Templates: Function template and class template, member function templates and template arguments, Exception Handling: syntax for exception handling code: try-catch- throw,MultipleExceptions.
ScritingLanguages:Overview of Scripting Languages – PERL, CGI, VB Script, Java Script.
PERL: Operators, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied Variables, Inter process Communication Threads, Compilation & Line Interfacing.

**Learning Outcomes:**

1. List common templates of functions, exception handling for embedded application. (L2)
2. Discuss about scripting languages in embedded development. (L2)

**Text Books:**


1. Michael J. Pont , "Embedded C", Pearson Education, 2nd Edition, 2008
2. Randal L. Schwartz, "Learning Perl", O"Reilly Publications, 6th Edition2011


**Reference Books:**


1. A. Michael Berman, "Data structures via C++", Oxford University Press,2002
2. Robert Sedgewick, "Algorithms in C++", Addison Wesley Publishing Company,1999
3. Abraham Silberschatz, Peter B, Greg Gagne, "Operating System Concepts", JohnWilley & Sons,2005Kaufmann.


**COURSE OUTCOMES VS POs MAPPING (**DETAILED; HIGH:3; MEDIUM:2; LOW:1**):**

| SNO | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 | PSO1 | PSO2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO.1** | 3 | 2 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 2 | - |
| **CO.2** | 3 | 2 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 2 | - |
| **CO.3** | 3 | 2 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 2 | - |
| **CO.4** | 3 | 2 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 2 | - |
| **CO.5** | 3 | 2 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 2 | - |
| **CO*** | 3 | 2 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 2 | - |

**** For Entire Course, PO & PSO Mapping***

| Subject Code | Subject Name | Hours | Credits |
|---|---|---|---|
| EC-ESVD1104.2 | System Design with Embedded Linux | 3 | 3 |

**Program Elective -II**

**Course Objectives:**

Faculty is going to

- Introduce embedded linux concepts and importance of POSIX standard.
- Provide the embedded linux architecture with its various subsystems.
- Understand the board support package design of a embedded board.
- What is porting of applications and real time linux.
- Use of templates and scripting language for program automation in embedded systems.

**Course Outcomes:**

At the end of this course, students will be able to

1. Discover the working of embedded 'C' and its implementation in a embedded system design. (L3)
2. Illustrate the importance of Object-Oriented Programming concepts for design of embedded systems. (L3)
3. Estimate the different components and their function of Board support package in a typical embedded design. (L2)
4. Review the porting of application feature and importance of real-time Linux.(L2)
5. Practice building, debugging and various components of a modern embedded linux with a case study. (L3)

**Unit-I:**

Embedded Linux , Vendor Independence, Time to Market,Varied Hardware Support, Open Source, Standards (POSIX®) Compliance, Embedded Linux Versus Desktop Linux, Embedded Linux Distributions, BlueCat Linux, Cadenux , Denx, Embedded Debian (Emdebian),ELinOS (SYSGO), Metrowerks ,MontaVista Linux, RTLinuxPro, TimeSys Linux.

**Learning Outcomes:**

1. Importance of Linux in design of OS for embedded systems. (L2)
2. Summarize the different POSIX standards and linux that support embedded architecture. (L2)

**Unit-II:**

Embedded Linux Architecture, Real-Time Executive, Monolithic Kernels, MicrokernelKernel Architecture – HAL, Memory manager, Scheduler, File System, I/O and Networking subsystem,IPC, User space, Start-up sequence, Boot Loader Phase, Kernel Start-Up, User SpaceInitialization.

**Learning Outcomes:**

1. Role of OOPs in design of embedded development. (L2)

**Unit-III:**

Board Support Package Embedded Storage: MTD, Architecture, Drivers, Embedded File System Embedded Drivers: Serial, Ethernet, I2C, USB, Timer, Kernel Modules.

**Learning Outcomes:**

1. Summarize the board support package and its components. (L2)
2. List the driver design for common peripherals like serial port, Ethernet, I2C, USB, Timers. (L2)

**Unit-IV:**

Porting Applications, Architectural Comparison, Application Porting Roadmap, Programming with Pthreads, Operating System Porting Layer (OSPL), Kernel API Driver, Real-Time Linux: Linux and Real time, Programming, Hard Real-time Linux

**Learning Outcomes:**

1. List the application porting functions. (L2)
2. Show the purpose and functioning of a real time Linux. (L2)

**Unit-V:**

Building and Debugging: Kernel, Building the Kernel, Building Applications, Building the Root File System, Integrated Development Environment, Debugging Virtual Memory Problems , Kernel Debuggers, Root file system Embedded Graphics. Graphics System, Linux Desktop Graphics, Embedded Linux Graphics, Embedded Linux Graphics Driver, Windowing Environments, Toolkits, and Applications,Case study of uClinux.

**Learning Outcomes:**

1. Explain the building and debugging process of kernel. (L2)
2. Perform a case study of uClinux for understanding the various features. (L2)

**Text Books:**


1. KarimYaghmour, "Building Embedded Linux Systems", O'Reilly &Associates
2. P Raghvan, Amol Lad, SriramNeelakandan, "Embedded Linux System Design and Development", AuerbachPublications


**Reference Books:**


1. Christopher Hallinan, "Embedded Linux Primer: A Practical Real WorldApproach",Prentice Hall, 2nd Edition,2010.
2. Derek Molloy, "Exploring BeagleBone: Tools and Techniques for Building withEmbedded Linux", Wiley, 1st Edition, 2014.


**COURSE OUTCOMES VS POs MAPPING (**DETAILED; HIGH:3; MEDIUM:2; LOW:1**):**

| SNO | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 | PSO1 | PSO2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO.1** | 3 | 2 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO.2** | 3 | 2 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO.3** | 3 | 2 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO.4** | 3 | 2 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO.5** | 3 | 2 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO*** | 3 | 2 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |

**** For Entire Course, PO & PSO Mapping***

| Subject Code | Subject Name | Hours | Credits |
|---|---|---|---|
| EC-ESVD1104.3 | CAD of Digital System | 3 | 3 |

**Program Elective -II**

**Course Objectives:**

Faculty is going to

- Understand the VLSI methodologies for design and fabrication of VLSI devices.
- Understand the fundamentals of CAD for VLSI design automationwith modeling, design, test and verification.
- Explain themethods of partitioning, floor planning, placement, routing for combinational optimization.
- Explain the simulation and synthesis for the design of VLSI circuits.
- Explain about multi-chip module and implementation of simple circuits with VHDL and Verilog programming.

**Course Outcomes:**

At the end of this course, students will be able to

1. Summarize the various methodologies for design and fabrication of VLSI devices. (L2)
2. Recognize the CAD tools for modelling, design, test and verification of VLSIsystems. (L2)
3. Illustrate the partitioning, floor planning, placement, routing methods for combinational optimization. (L2)
4. Demonstrate the CAD tools like simulation and synthesis at different abstract layers of VLSI design. (L3)
5. Interpret the importance of Multi-Chip Modules and various HDL programming for VLSI design. (L3)

**Unit-I:**Introduction to VLSI Methodologies – Design and Fabrication of VLSI Devices, Fabrication Materials, Transistor Fundamentals, Fabrication of VLSI Circuits, Design Rules Layout of Basic Devices, Fabrication Process and its Impact on Physical Design, Scaling Methods, Status of Fabrication Process, Issues related to the Fabrication Process, Future of Fabrication Process, Solutions for Interconnect Issues, Tools for Process Development

**Learning Outcomes:**

1. Explain the fabrication process and design rules of VLSI. (L2)
2. Explain impact of scaling, interconnect issues in VLSI. (L2)
3. List the tools for the VLSI process development. (L2)

**Unit-II:** VLSI design automation tools – Data Structures and Basic Algorithms, Basic Terminology, Complexity Issues and NP-hardness, Basic Algorithms, Basic Data Structures, graph theory and Computational complexity, tractable and intractable problems.

**Learning Outcomes:**

1. Provide the VLSI design automation tools for various improvements. (L2)

**Unit-III:**General purpose methods for combinational optimization – **Partitioning-** Problem Formulation, Classification of Partitioning Algorithms, Group Migration Algorithms , Simulated Annealing Simulated Evolution, Other Partitioning Algorithms Performance Driven Partitioning **Floor planning**- Chip planning , Pin Assignment , Integrated Approach, **Placement**- Problem Formulation , Classification of Placement Algorithms, Simulation Based Placement Algorithms , Partitioning Based Placement Algorithms , Performance Driven Placement, **Routing -**Global Routing, , Problem Formulation , Classification of Global Routing Algorithms, Maze Routing Algorithms , Line-Probe Algorithms, Shortest Path Based Algorithms.

Steiner Tree based Algorithms Integer Programming Based Approach , Performance Driven Routing

**Learning Outcomes:**

1. Classification of partitioning methods. (L2)
2. Summarize floor planning process. (L2)
3. Apply various routing algorithms for optimization in VLSI circuits. (L3)

**Unit-IV:Simulation-** Gate-level Modeling and Simulation, Switch-level Modeling and Simulation, **Logic Synthesis and Verification -** Introduction to Combinational Logic Synthesis , Binary-decision Diagrams, Two-level Logic Synthesis, **High-level Synthesis-** Hardware Models for High level Synthesis , Internal Representation of the Input Algorithm , Allocation, Assignment and Scheduling

**Learning Outcomes:**

1. Explain the simulation methods for various abstract levels of VLSI. (L3)
2. Demonstrate the various synthesis models for VLSI circuit verification. (L3)

**Unit-V:**MCMs-VHDL-Verilog-implementation of simple circuits using VHDL.

**Learning Outcomes:**

1. Implementation of simpler circuits using VHDL and Verilog HDL languages. (L3)
2. Discuss the working of a multi-chip module as a VLSI circuit. (L2)

**Text Books:**


1. N.A. Sherwani, "Algorithms for VLSI Physical DesignAutomation".
2. S.H. Gerez, "Algorithms for VLSI DesignAutomation.


**COURSE OUTCOMES VS POs MAPPING (**DETAILED; HIGH:3; MEDIUM:2; LOW:1**):**

| SNO | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 | PSO1 | PSO2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO.1** | 3 | 2 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO.2** | 3 | 2 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO.3** | 3 | 2 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO.4** | 3 | 2 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO.5** | 3 | 2 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO*** | 3 | 2 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |

**** For Entire Course, PO & PSO Mapping***

| Subject Code | Subject Name | Hours | Credits |
|---|---|---|---|
| EC-ESVD1105.1 | IOT and its Applications | 3 | 3 |

**Program Elective-III**

**Course Objectives:**

Faculty is going to

- Explain the fundamentals of IoT concepts.
- List the IoT networking protocols.
- Provide various platforms based IoT design and development.
- Understand the Data analytics for IoT decision making and various supporting services utilized in a typical IoT.
- List various applications and case studies of IoT.

**Course Outcomes:**

At the end of this course, students will be able to

1. Apply the Knowledge in IOT Technologies and Datamanagement. (L3)
2. Determine the values chains Perspective of M2M toIOT. (L2)
3. Implement the state of the Architecture of anIOT. (L2)
4. Compare IOT Applications in Industrial & realworld. (L4)
5. Demonstrate knowledge and understanding the security and ethical issues of anIOT. (L3)

**UNIT-I:FUNDAMENTALS OF IoT-** Evolution of Internet of Things, Enabling Technologies, IoT Architectures,oneM2M, IoT World Forum (IoTWF) and Alternative IoT models, Simplified IoT Architecture and Core IoT Functional Stack, Fog, Edge and Cloud in IoT, Functional blocks of an IoT ecosystem, Sensors, Actuators, Smart Objects and Connecting Smart Objects.

IoT Platform overview: Overview of IoT supported Hardware platforms such as: Raspberry pi, ARM Cortex Processors, Arduino and Intel Galileo boards.

**Learning Outcomes:**

1. Show the IoT architecture and core functions. (L2)
2. Describe the functional blocks of sensors and actuators. (L2)
3. List the common IoT platforms like Arduino, Intel Galileo and raspberry pi. (L2)

**UNIT-II:IoT PROTOCOLS-** IT Access Technologies: Physical and MAC layers, topology and Security of IEEE 802.15.4, 802.15.4g, 802.15.4e, 1901.2a, 802.11ah and Lora WAN, Network Layer: IP versions, Constrained Nodes and Constrained Networks, Optimizing IP for IoT: From 6LoWPAN to 6Lo, Routing over Low Power and Lossy Networks, Application Transport Methods: Supervisory Control and Data Acquisition, Application Layer Protocols: CoAP and MQTT.

**Learning Outcomes:**

1. List and understand various MAC level protocols used in IoT. (L2)
2. Provide overview of 6LoWPAN, Lora WAN network protocols. (L2)
3. Explain the application transport methods like CoAP and MQTT. (L2)

**UNIT-III: DESIGN AND DEVELOPMENT-** Design Methodology, Embedded computing logic, Microcontroller, System on Chips, IoT system building blocks, Arduino, Board details, IDE programming, Raspberry Pi, Interfaces and Raspberry Pi with Python Programming.

**Learning Outcomes:**

1. Explain the design methodology for a typical IoT platform. (L2)
2. Provide programming and diagrams for development of Arduino and raspberry pi based systems.

(L3)

**UNIT-IV: DATA ANALYTICS AND SUPPORTING SERVICES-** Structured Vs Unstructured Data and Data in Motion Vs Data in Rest, Role of Machine Learning – No SQL Databases, Hadoop Ecosystem, Apache Kafka, Apache Spark, Edge Streaming Analytics and Network Analytics, Xively Cloud for IoT, Python Web Application Framework, Django, AWS for IoT, System Management with NETCONF-YANG.

**Learning Outcomes:**

1. List the supporting services like SQL databases, Edge streaming, network analytics etc. (L3)
2. Summarize about the applications like AWS, python web framework-Django, Hadoop etc. (L2)

**UNIT-V: CASE STUDIES/INDUSTRIAL APPLICATIONS:** IoT applications in home, infrastructures, buildings, security, Industries, Home appliances, other IoT electronic equipment's. Use of Big Data and Visualization in IoT, Industry 4.0 concepts.

Sensors and sensor Node and interfacing using any Embedded target boards (Raspberry Pi / Intel Galileo/ARM Cortex/ Arduino)

**Learning Outcomes:**

1. List the applications and case study of IoT in various domains. (L2)
2. Show the sensor node and interfacing with embedded target boards. (L3)

**Text Books:**


1. IoT Fundamentals: Networking Technologies, Protocols and Use Cases for Internet of Things, David Hanes, Gonzalo Salgueiro, Patrick Grossetete, Rob Barton and Jerome Henry, Cisco Press, 2017


**Reference Books:**


1. Internet of Things – A hands-on approach, ArshdeepBahga, Vijay Madisetti, Universities Press,2015
2. The Internet of Things – Key applications and Protocols, Olivier Hersent, David Boswarthick, Omar Elloumi and Wiley, 2012 (for Unit-II).
3. "From Machine-to-Machine to the Internet of Things – Introduction to a New Age of Intelligence",Jan Ho¨ ller, VlasiosTsiatsis, Catherine Mulligan, Stamatis, Karnouskos, Stefan Avesand. David Boyle and Elsevier, 2014.
4. Architecting the Internet of Things,Dieter Uckelmann, Mark Harrison, Michahelles and Florian (Eds), Springer,2011.
5. Recipes to Begin, Expand, and Enhance Your Projects, 2nd Edition,Michael Margolis, Arduino Cookbook and O"Reilly Media,2011.


**COURSE OUTCOMES VS POs MAPPING (**DETAILED; HIGH:3; MEDIUM:2; LOW:1**):**

| SNO | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 | PSO1 | PSO2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO.1** | 3 | 2 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO.2** | 3 | 2 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO.3** | 3 | 2 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO.4** | 3 | 2 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO.5** | 3 | 2 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO*** | 3 | 2 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |

**** For Entire Course, PO & PSO Mapping***

| Subject Code | Subject Name | Hours | Credits |
|---|---|---|---|
| EC-ESVD1105.2 | Hardware Software Co-Design | 3 | 3 |

**Program Elective-III**

**Course Objectives:**

Faculty is going to

- list the issues and synthesis in co-design of hardware and software.
- Provide prototyping and emulation process of a typical co-design system.
- Show the process with in a embedded processor development environment.
- Provide the design specification and verification of the co-design.
- Give the system level specification and design of a typical hardware software codesign.

**Course Outcomes:**

At the end of this course, students will be able to

1. Identify the issues in co-design and synthesis algorithms to overcome. (L2)
2. Summarize the target architecture, prototyping and emulation of a given architecture for co-design. (L2)
3. Illustrate the compilation process and IDE for embedded software development. (L3)
4. Recognize the co-design models for design and verification in a co-design system. (L2)
5. Identify the languages for system level specification and design with case study. (L2)

**UNIT-I:**

**Co- Design Issues**

Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

**Co- Synthesis Algorithms**

Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

**Learning Outcomes:**

1. Importance of co-design and architecture. (L2)
2. Methodology to synthesis the hardware-software partitioning. (L2)

**UNIT-II:**

**Prototyping and Emulation**

Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

**Target Architectures**

Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), MixedSystems.

**Learning Outcomes:**

1. Techniques to prototype and emulate the system architecture. (L2)
2. Understanding different embedded architectures for control design. (L2)

**UNIT-III:**

**Compilation Techniques and Tools for Embedded Processor Architectures**

Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

**Learning Outcomes:**

1. Explain the compilation process for a processor architecture. (L2)

2. Examine the software development needs for embedded development. (L2)

**UNIT-IV:**

**Design Specification and Verification**

Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools,Interface verification.

**Learning Outcomes:**

1. Co-design computational models and concurrent computations. (L2)
2. Provide verification and design specifications of the computational model. (L2)

**UNIT-V:**

**Languages for System-Level Specification and Design-I**

System-level specification, design representation for system level synthesis, system level specification languages.

**Languages for System-Level Specification and Design-II**

Heterogeneous specifications and multi-language co-simulation, the cosyma system and lycos system.

**Learning Outcomes:**

1. Discussion of system level specification and design and languages that provide the modeling. (L2)
2. Multilanguage co-simulation and specifications within embedded systems. (L3)

**Text Books:**


1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – 2009, Springer.
2. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, 2002, Kluwer AcademicPublishers.


**Reference Books:**


1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - 2010 – Springer Publications.


**COURSE OUTCOMES VS POs MAPPING (**DETAILED; HIGH:3; MEDIUM:2; LOW:1**):**

| SNO | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 | PSO1 | PSO2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO.1** | 3 | 2 | 2 | 2 | 2 | - | - | - | - | 2 | - | 1 | 1 | - |
| **CO.2** | 3 | 2 | 2 | 2 | 2 | - | - | - | - | 2 | - | 1 | 1 | - |
| **CO.3** | 3 | 2 | 2 | 2 | 2 | - | - | - | - | 2 | - | 1 | 1 | - |
| **CO.4** | 3 | 2 | 2 | 2 | 2 | - | - | - | - | 2 | - | 1 | 1 | - |
| **CO.5** | 3 | 2 | 2 | 2 | 2 | - | - | - | - | 2 | - | 1 | 1 | - |
| **CO*** | 3 | 2 | 2 | 2 | 2 | - | - | - | - | 2 | - | 1 | 1 | - |

**** For Entire Course, PO & PSO Mapping***

| Subject Code | Subject Name | Hours | Credits |
|---|---|---|---|
| EC-ESVD1105.3 | Artificial Intelligence | 3 | 3 |

**Program Elective-III**

**Course Objectives:**

Faculty is going to

- Understand the concept of Artificial Intelligence, search techniques andknowledge representationissues.
- Understanding reasoning and fuzzy logic for artificialintelligence.
- Understanding game playing and natural languageprocessing.

**Course Outcomes:**

At the end of course, students are able to

1. Demonstrate fundamental understanding of the evaluation of Artificial Intelligence (AI) and its foundations. (L3)
2. Apply basic principles of AI in solutions that require problem solving, perception, knowledge representation, and learning. (L3)
3. Design experiments with various AI concepts and analyze results. (L2)
4. Show the importance of artificial intelligence and planning in solving real world problems. (L3)
5. Create interactive and rational system using appropriate learning techniques also, to measure the level of user satisfaction and efficiency of the expert system and ANN. (L3)

**Unit-I**

What is AI (Artificial Intelligence)? : The AI Problems, The Underlying Assumption, What are A Techniques, The Level Of The Model, Criteria For Success, Some General References, One Final Word Problems, State Space Search & Heuristic Search Techniques: Defining The Problems As A State Space Search, Production Systems, Production Characteristics, Production System Characteristics, And Issues In The Design Of Search Programs, Additional Problems. Generate-And-Test, Hill Climbing, Best-First Search, Problem Reduction, Constraint Satisfaction, Means-Ends Analysis.

**Learning Outcomes:**

1. AI and the levels of model with some general references. (L2)
2. Defining the problems of state space, search and production systems with various models. (L3)

**Unit-II**

Knowledge Representation Issues: Representations And Mappings, Approaches To Knowledge Representation. Using Predicate Logic: Representation Simple Facts In Logic, Representing Instance And Isa Relationships, Computable Functions And Predicates, Resolution. Representing Knowledge Using Rules: Procedural Versus Declarative Knowledge, Logic Programming, Forward Versus Backward Reasoning.

**Learning Outcomes:**

1. Understand representations and relationship using various logic methods. (L2)
2. Understanding representation of knowledge using rules with various models. (L3)

**Unit-III**

Symbolic Reasoning Under Uncertainty: Introduction To No monotonic Reasoning, Logics For Non-monotonic Reasoning. Statistical Reasoning: Probability And Bays‟ Theorem, Certainty Factors And Rule-Base Systems, Bayesian Networks, Dempster Shafer Theory.

Fuzzy Logic. Weak Slot-and-Filler Structures: Semantic Nets, Frames. Strong Slot-and-Filler Structures: Conceptual Dependency, Scripts, CYC

**Learning Outcomes:**

1. Summarize the symbolic reasoning and different systems of certainty. (L2)

2. Understand the need of fuzzy logic with various representation models. (L3)

**Unit-IV**

Game Playing: Overview, And Example Domain: Overview, Mini Max, Alpha-Beta Cut-off, Refinements, Iterative deepening, The Blocks World, Components Of A Planning System, Goal Stack Planning, Nonlinear Planning Using Constraint Posting, Hierarchical Planning, Reactive Systems, Other Planning Techniques. Understanding: What is understanding? What makes it hard? As constraint satisfaction

**Learning Outcomes:**

1. Discuss the components of a planning systems. (L2)
2. List the importance of reactive systems and various planning techniques. (L3)

**Unit-V**

Natural Language Processing: Introduction, Syntactic Processing, Semantic Analysis, Semantic Analysis, Discourse And Pragmatic Processing, Spell Checking Connectionist Models: Introduction: Hopfield Network, Learning In Neural Network, Application Of Neural Networks, Recurrent Networks, Distributed Representations, Connectionist AI And Symbolic AI.

**Learning Outcomes:**

1. Illustrate the importance and elements of natural language processing. (L2)
2. Demonstrate the spell-checking connectionist models and their application. (L3)

**TextBooks:**


1. Elaine Rich and Kevin Knight "Artificial Intelligence", 2nd Edition, Tata Mcgraw-Hill,2005.
2. Stuart Russel and Peter Norvig, "Artificial Intelligence: A Modern Approach",3rdEdition, Prentice Hall,2009.


**COURSE OUTCOMES VS POs MAPPING (**DETAILED; HIGH:3; MEDIUM:2; LOW:1**):**

| SNO | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 | PSO1 | PSO2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO.1** | 3 | 2 | 2 | 2 | 3 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO.2** | 3 | 2 | 2 | 2 | 3 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO.3** | 3 | 2 | 2 | 2 | 3 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO.4** | 3 | 2 | 2 | 2 | 3 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO.5** | 3 | 2 | 2 | 2 | 3 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO*** | 3 | 2 | 2 | 2 | 3 | - | - | - | - | 2 | - | 2 | 1 | - |

**** For Entire Course, PO & PSO Mapping***

| Subject Code | Subject Name | Hours | Credits |
|---|---|---|---|
| EC-ESVD1106 | Research Methodology and IPR | 3 | 3 |

**Course Objectives:**

- What is research problem formulation?
- How to analyze research information.
- What are the research ethics
- How IPR works.
- How to protect IPR and for economic growth.

**Course Outcomes:**

At the end of this course, students will be able to

1. Analyze research relatedinformation. (L4)
2. Follow researchethics. (L3)
3. Understandthattoday"sworldiscontrolledbyComputer,InformationTechnology,but tomorrow world will be ruled by ideas, concept, andcreativity. (L2)
4. Understanding that when IPR would take such important place in growth of individuals &nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering inparticular. (L2)
5. Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits. (L2)

**Unit-I:** Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of
research problem. Approaches of investigation of solutions for research problem, datacollection, analysis, interpretation, Necessaryinstrumentations

**Learning Outcomes:**

1. Discuss the various characteristics of a research problem. (L2)
2. Demonstrate various approaches of investigation for solving research problems. (L3)

**Unit-II:** Effective literature studies approaches, analysis Plagiarism, Research ethics.Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a reviewcommittee

**Learning Outcomes:**

1. Discuss the importance of plagiarism and research ethics. (L2)
2. Demonstrate the way of preparing technical writing for various purposes. (L3)

**Unit-III:** Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

**Learning Outcomes:**

1. Explain the importance of intellectual property and its rights. (L2)
2. Explain the patenting and development process. (L2)

**Unit-IV:** Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications.

**Learning Outcomes:**

1. Examine the scope and working of patent rights. (L2)

**Unit-V:** New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

**Text Books:**


1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science& engineeringstudents""
2. Wayne Goddard and Stuart Melville, "Research Methodology: AnIntroduction"
3. Ranjit Kumar, 2nd Edition , "Research Methodology: A Step by Step Guide forbeginners"
4. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd,2007.


**Reference Books:**


1. Mayall , "Industrial Design", McGraw Hill,1992.
2. Niebel , "Product Design", McGraw Hill,1974.
3. Asimov , "Introduction to Design", Prentice Hall,1962.
4. Robert P. Merges, Peter S. Menell, Mark A. Lemley, " Intellectual Property inNew
5. Technological Age",2016.
6. T. Ramappa, "Intellectual Property Rights Under WTO", S. Chand,2008


**COURSE OUTCOMES VS POs MAPPING (**DETAILED; HIGH:3; MEDIUM:2; LOW:1**):**

| SNO | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 | PSO1 | PSO2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO.1** | 3 | 2 | 2 | 2 | 3 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO.2** | 3 | 2 | 2 | 2 | 3 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO.3** | 3 | 2 | 2 | 2 | 3 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO.4** | 3 | 2 | 2 | 2 | 3 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO.5** | 3 | 2 | 2 | 2 | 3 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO*** | 3 | 2 | 2 | 2 | 3 | - | - | - | - | 2 | - | 2 | 1 | - |

**** For Entire Course, PO & PSO Mapping***

| Subject Code | Subject Name | Hours | Credits |
|---|---|---|---|
| EC-ESVD1107 | RTL Simulation and Synthesis with PLDs Lab | 4 | 2 |

## RTL Simulation and Synthesis with PLDs Lab

Note: Use EDA tools like Cadence, Mentor Graphics andXilinx.

**Course Objectives:**

Faculty is providing simulations of :

- Show the different digital circuits in Verilog modeling for simple applications in a computer.
- Demonstration Verilog models for memory systems and signal processing.

**Course Outcomes:**

At the end of the laboratory work, students will be able to:

1. Demonstrate the working design of common combinational circuits in Verilog modeling. (L3)
2. Illustrate various arithmetic circuits in Verilog used in computational circuits. (L3)
3. Develop state machines for implementation of counters and other applications. (L3)
4. Demonstrate the Verilog models of different memory system-based modules. (L3)
5. Implement the basic models related to signal processing implementation within a digital system. (L3)

**List of Experiments:**

1. Verilog implementationof 8:1 Mux/Demux.
2. Verilog implementationof Full Adder.
3. Verilog implementationof 8-bit Magnitudecomparator.
4. Verilog implementationof Paritygenerator.
5. Verilog implementation of Arithmetic circuits like serial adder/ subtractor,parallel adder/subtractor, serial/parallelmultiplier.
6. Verilog implementationof 3-bit SynchronousCounters.
7. Sequence generator/detectors, Synchronous FSM – Mealy and Mooremachines.
8. Vending machines - Traffic Light controller, ATM, elevatorcontrol.
9. PCI Bus & arbiter and downloading onFPGA.
10. UART/ USART implementation inVerilog.
11. Realization of single port SRAM inVerilog.
12. Discrete Fourier transform/Fast Fourier Transform algorithm inVerilog.

**COURSE OUTCOMES VS POs MAPPING (**DETAILED; HIGH:3; MEDIUM:2; LOW:1**):**

| SNO | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 | PSO1 | PSO2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CO.1 | 3 | 2 | 2 | 2 | 3 | - | - | - | 2 | 2 | - | 2 | 1 | - |
| CO.2 | 3 | 2 | 2 | 2 | 3 | - | - | - | 2 | 2 | - | 2 | 1 | - |
| CO.3 | 3 | 2 | 2 | 2 | 3 | - | - | - | 2 | 2 | - | 2 | 1 | - |
| CO.4 | 3 | 2 | 2 | 2 | 3 | - | - | - | 2 | 2 | - | 2 | 1 | - |
| CO.5 | 3 | 2 | 2 | 2 | 3 | - | - | - | 2 | 2 | - | 2 | 1 | - |
| CO* | 3 | 2 | 2 | 2 | 3 | - | - | - | 2 | 2 | - | 2 | 1 | - |

**** For Entire Course, PO & PSO Mapping***

| Subject Code | Subject Name | Hours | Credits |
|---|---|---|---|
| EC-ESVD1107 | Microcontrollers and Programmable Digital Signal Processors Lab | 4 | 2 |

**Course Objectives:**

Faculty is providing simulations of:

- Core SoC and DSPprocessor functions.
- Develop prototype codes using commonly available on and off chip peripherals onthe Cortex M3 and DSP developmentboards.

**Course Outcomes:**

At the end of the laboratory work, students will be able to:

1. Demonstrate the implementation of basic interfaces to a ARM cortex-M3 development system. (L3)
2. Illustrate the common functions of timers, ADC, watchdog in the ARM systems. (L3)
3. Prepare models using serial communication, PWM, sleep modes and audio signals of a ARM system. (L3)
4. Implement basic DSP functions in a DSP6713 using assembly and C programming. (L3)
5. Make use of convolution and filters for signal enhancement in DSP systems. (L3)

**List of Experiments:**

**Part A)** Experiments to be carried out on Cortex-M3 development boards and using GNU Tool chain

1. Blink an LED with software delay, delay generated using the Sys Ticktimer.
2. Control an LED using switch by polling method, by interrupt method and flash the LEDonce every five switchpresses.
3. Temperature indication on an RGBLED.
4. UART EchoTest.
5. System clock real time alteration using the PLLmodules.
6. Take analog readings on rotation of rotary potentiometer connected to an ADCchannel.
7. Control intensity of an LED using PWM implemented in software andhardware.
8. Mimic light intensity sensed by the light sensor by varying the blinking rate of anLED.
9. Evaluate the various sleep modes by putting core in sleep and deep sleepmodes.
10. System reset using watchdog timer in case something goeswrong.
11. Sample sound using a microphone and display sound levels onLEDs.

**Part B)** Experiments to be carried out on DSP C6713 evaluation kits and using Code Composer Studio (CCS)

1. To develop an assembly code and C code to compute Euclidian distance between anytwo points.
2. To develop assembly code and study the impact of parallel, serial and mixedexecution.
3. To develop assembly and C code for implementation of convolutionoperation.
4. To design and implement filters in C to enhance the features of given inputsequence/signal.

**COURSE OUTCOMES VS POs MAPPING (**DETAILED; HIGH:3; MEDIUM:2; LOW:1**):**

| SNO | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 | PSO1 | PSO2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CO.1 | 3 | 2 | 2 | 2 | 2 | - | - | - | 2 | 2 | - | 2 | 1 | - |
| CO.2 | 3 | 2 | 2 | 2 | 2 | - | - | - | 2 | 2 | - | 2 | 1 | - |
| CO.3 | 3 | 2 | 2 | 2 | 2 | - | - | - | 2 | 2 | - | 2 | 1 | - |
| CO.4 | 3 | 2 | 2 | 2 | 2 | - | - | - | 2 | 2 | - | 2 | 1 | - |
| CO.5 | 3 | 2 | 2 | 2 | 2 | - | - | - | 2 | 2 | - | 2 | 1 | - |
| CO* | 3 | 2 | 2 | 2 | 2 | - | - | - | 2 | 2 | - | 2 | 1 | - |

**** For Entire Course, PO & PSO Mapping***

| Subject Code | Subject Name | Hours | Credits |
|---|---|---|---|
| EC-ESVD1201 | Analog and Digital CMOS VLSI Design | 3 | 3 |

**Course objectives:**

- To teach fundamentals of CMOS Digital integrated circuit design such as importance of Combinational MOS logic circuits, and Sequential MOS logiccircuits.
- To teach the fundamentals of Dynamic logic circuits and basic semiconductor memories which are the basics for the design of high performance digital integratedcircuits.
- Basic design concepts, issues and tradeoffs involved in analog IC design areexplored.
- To learn about Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power Supply Rejection Ratio of Two-Stage Op Amps, Cascade Op Amps, Measurement Techniques of OP Amp.

**Course Outcomes:**

At the end of this course, students will be able to

1. Appreciate the trade-offs involved in analog integrated circuitdesign. (L2)
2. Understand and appreciate the importance of noise and distortion in analogcircuits. (L2)
3. Analyze complex engineering problems critically in the domain of analog IC design for conductingresearch. (L4)
4. Demonstrate advanced knowledge in Static and dynamic characteristics of CMOS, Alternative. (L3)
5. Solve engineering problems for feasible and optimal solutions in the core area of digitalICs. (L3)

**Syllabus Contents:**

Technology Scaling and Road map, Scaling issues, Standard 4 mask NMOS Fabrication process

**Digital CMOS Design:**

**Unit-I:** Review: Basic MOS structure and its static behavior, Quality metrics of a digital design: Cost, Functionality, Robustness, Power, and Delay, Stick diagram and Layout, Wire delay models. Inverter: Static CMOS inverter, Switching threshold and noise margin concepts and their Evaluation, Dynamic behavior, Power consumption.

**Learning Outcomes:**

1. Examine the CMOS design and its inverter function. (L2)

**Unit-II:** Physical design flow: Floor planning, Placement, Routing, CTS, Power analysis and IR drop estimation-static and dynamic, ESD protection-human body model, Machine model.

Combinational logic: Static CMOS design, Logic effort, Rationed logic, Pass transistor logic, Dynamic logic, Speed and power dissipation in dynamic logic, Cascading dynamic gates, CMOS transmission gate logic.

**Learning Outcomes:**

1. Understand the physical design flow in a typical cmos systems. (L2)
2. Demonstrate various CMOS factors in designing the combinational logic systems. (L3)

**Unit-III:**Sequential logic: Static latches and registers, Bi-stability principle, MUX based latches,

Static SR flip-flops, Master-slave edge-triggered register, Dynamic latches and registers, Concept of pipelining, Pulse registers, Non-bistable sequential circuit. Advanced technologies: Giga-scale dilemma, Short channel effects, High–k, Metal Gate Technology, FinFET, TFET etc.

**Learning Outcomes:**

1. Demonstrate the working of different sequential circuits using CMOS design. (L3)
2. Summarize the advanced technologies that are trending and shaping the future. (L2)

**Analog CMOS Design:**

**Unit-IV:** Single Stage Amplifier: CS stage with resistance load, Divide connected load, Current source load, Triode load, CS stage with source degeneration, Source follower, Common gate stage, Cascade stage, Choice of device models. Differential Amplifiers: Basic difference pair, Common mode response, Differential pair with MOS loads, Gilbert cell.

**Learning Outcomes:**

1. Demonstrate different Analog CMOS circuits and their working. (L2)

**Unit-V:** Passive and active current mirrors: Basic current mirrors, Cascade mirrors, Active current mirrors. Frequency response of CS stage: Source follower, Common gate stage, Cascade stage and difference pair, Noise. Operational amplifiers: One stage OPAMP, Two stage OPAMP, Gain boosting, Common mode feedback, Slew rate, PSRR, Compensation of 2 stage OPAMP

**Learning Outcomes:**

1. Examine the working of analog CMOS designs. (L2)

**Text Books:**


1. J P Rabaey, A P Chandrakasan, B Nikolic, "Digital Integrated circuits: A design perspective", Prentice Hall electronics and VLSI series, 2ndEdition.
2. Baker, Li, Boyce, "CMOS Circuit Design, Layout, and Simulation", Wiley, 2ndEdition.
3. BehzadRazavi , "Design of Analog CMOS Integrated Circuits", TMH,2007.


**Reference Books:**


1. Phillip E. Allen and Douglas R. Holberg, "CMOS AnalogCircuit Design",Oxford, 3rd Edition.
2. R J Baker, "CMOS circuit Design, Layout and Simulation", IEEE Inc.,2008.
3. Kang, S. and Leblebici, Y., "CMOS Digital Integrated Circuits, Analysis and Design",TMH, 3rdEdition.
4. Pucknell, D.A. and Eshraghian, K., "Basic VLSI Design", PHI, 3rdEdition.


**COURSE OUTCOMES VS POs MAPPING (**DETAILED; HIGH:3; MEDIUM:2; LOW:1**):**

| SNO | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 | PSO1 | PSO2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO.1** | 3 | 2 | 2 | 2 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO.2** | 3 | 2 | 2 | 2 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO.3** | 3 | 2 | 2 | 2 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO.4** | 3 | 2 | 2 | 2 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO.5** | 3 | 2 | 2 | 2 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO*** | 3 | 2 | 2 | 2 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |

**** For Entire Course, PO & PSO Mapping***

| Subject Code | Subject Name | Hours | Credits |
|---|---|---|---|
| EC-ESVD1202 | REAL TIME OPERATING SYSTEMS | 3 | 3 |

**Course Objectives:**

- To Know the Basic Designs using anRTOS.
- To Know the Functions and Types of RTOS for EmbeddedSystems.
- To Analyze the issues in real time operatingsystems
- To Study the Programming Concepts of RTLinux.
- To Understand Applications Control by RT LinuxSystem.
- To Analyze the Operating SystemSoftware

**Course Outcomes**

Upon the completion of the course student will be able to

1. Apply task based RTOS functions to implement embeddedapplications. (L3)
2. Demonstrate the semaphore and message queues. (L3)
3. Summarize the functioning of interrupts, exceptions and timers in a typical RTOS. (L3)
4. Illustrate the working of memory management in RTOS. (L3)
5. Discuss the synchronization and communication of processes in RTOS. (L2)

**UNIT I**

**Introduction to Real-Time Operating Systems -** Defining an RTOS, The scheduler, Kernel Objects and services, Key characteristics of an RTOS

**Task-** Defining a Task, Task States and Scheduling, Typical Task Operations, Typical Task Structure, Synchronization, Communication and Concurrency

**Learning Outcomes:**

1. Provide different task operations in RTOS. (L2)
2. Extend the task function for synchronization and communication concurrency. (L3)

**UNIT II**

**Semaphores -** Defining Semaphores, Typical Semaphore Operations, Typical Semaphore Use

**Message Queues -** Defining Message Queues, Message Queue States, Message Queue Content, Message Queue Storage, Typical Message Queue Operations, Typical Message Queue Use, Pipes, Event Registers, Signals and conditionVariables

**Learning Outcomes:**

1. Utilize semaphores to perform task synchronization. (L2)
2. Provide message queues for task management functions. (L3)

**UNIT III**

**Exceptions and Interrupts -** Exceptions and Interrupts, Applications of Exceptions and Interrupts, Closer look at exceptions and interrupts, processing general Exceptions, Nature of Spurious Interrupts

**Timer and Timer Services -** Real-Time clocks and System Clocks, Programmable Interval Timers, Timer Interrupt Service Routines.

**I/O Subsystems -** I/O concepts, I/O subsystems.

**Learning Outcomes:**

1. Summarize the interrupt and exception functions in a RTOS. (L3)
2. Demonstrate the timer services and IO subsystem functions of RTOS. (L3)

**UNIT IV**

**Memory Management -** Dynamic Memory Allocation in Embedded Systems, Fixed-Size Memory management in Embedded Systems, Blocking VS. Non-Blocking Memory Functions, Hardware Memory Management Units

**Modularizing an application for concurrency-** An outside-in approach to decompose Applications, Guidelines and Recommendations for Identifying Concurrency, Schedulable Analysis.

**Learning Outcomes:**

1. Discuss the memory management functions in RTOS. (L2)
2. Extend the functions of RTOS to modularize for concurrency. (L2)

**UNIT V**

**Synchronization and Communication -** Synchronization, Communication, Resource Synchronization Methods, Critical section, Common practical design patterns, Specific Solution Design Patterns, **Common Design Problems -** Resource Classification, Deadlocks, Priority Inversion.

**Learning Outcomes:**

1. Provide the synchronization and communication problems for RTOS. (L2)

**Text Books**

1. Qing Li, Caroline Yao (2003), "Real-Time Concepts for Embedded Systems", CMP Books.

**Reference Books**

1. AlbertCheng,(2002),"Real-Time Systems: Scheduling, Analysis and Verification",WileyInterscience.
2. HermannKopetz, (1997), "Real-Time Systems: Design Principlesfor Distributed Embedde Applications",Kluwer.
3. InsupLee,JosephLeung,andSangSon,(2008)"HandbookofReal-TimeSystems",
4. Chapman aHall.Krishna and Kang G Shin, (2001), "Real-Time Systems", McGrawHill.

**COURSE OUTCOMES VS POs MAPPING (**DETAILED; HIGH:3; MEDIUM:2; LOW:1**):**

| SNO | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 | PSO1 | PSO2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO.1** | 3 | 2 | 2 | 2 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO.2** | 3 | 2 | 2 | 2 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO.3** | 3 | 2 | 2 | 2 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO.4** | 3 | 2 | 2 | 2 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO.5** | 3 | 2 | 2 | 2 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO*** | 3 | 2 | 2 | 2 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |

**** For Entire Course, PO & PSO Mapping***

| Subject Code | Subject Name | Hours | Credits |
|---|---|---|---|
| EC-ESVD1203.1 | Memory Architectures | 3 | 3 |

**Program Elective-IV**

**Course Objectives:**

Faculty is going to

- Understand the various SRAM technologies available for memory systems.
- Understand the various DRAM technologies available for memory systems.
- List the ROM technologies for design of memory modules.
- Understand the fault models and their impact on memory technologies.
- Show the latest trends in memory design and applications.

**Course Outcomes:**

At the end of the course, students will be able to:

1. Distinguish different SRAM technologies for design of memory systems. (L3)
2. Distinguish different DRAM technologies for design of memory systems. (L3)
3. Summarize the various non-volatile ROM technology working for memory design. (L3)
4. Identify various fault models, modes and mechanisms in semiconductor memoriesand their testingprocedures. (L2)
5. Summarize the state-of-the-art memory chipdesign for modern computing systems. (L2)

**Unit-I:**Random Access Memory Technologies:
Static Random-Access Memories (SRAMs), SRAM Cell Structures, MOS SRAMArchitecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, Advanced SRAM Architectures, Application Specific SRAMs.

**Learning Outcomes:**

1. SRAM as a memory cell and the peripheral connect circuit. (L2)
2. Bipolar SRAM as a newer trend and its applications. (L2)

**Unit-II:**DRAMs, MOS DRAM Cell, BiCMOS DRAM, Error Failures in DRAM, AdvancedDRAM Design and Architecture, Application Specific DRAMs. SRAM and DRAM Memory controllers.

**Learning Outcomes:**

1. Understand the DRAM cell function along with operations. (L2)
2. Summarize the design of BICMOS DRAM cell design. (L2)

**Unit-III:** Non-Volatile Memories: Masked ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Non-volatile SRAM, Flash Memories.

**Learning Outcomes:**

1. List the ROM models available for the non-volatile data storage. (L2)
2. NVRAM and flash memory as the forefront of memory technologies and their application in embedded systems. (L2)

**Unit-IV:**Semiconductor Memory Reliability and Radiation Effects: General Reliability Issues, RAM Failure Modes and Mechanism, Nonvolatile Memory, Radiation Effects, SEP, Radiation Hardening Techniques. Process and Design Issues, Radiation Hardened Memory Characteristics, Radiation Hardness Assurance and Testing.

**Learning Outcomes:**

1. Summarize the importance of memory reliability and their measure. (L2)

2. Explain the radiation effects and the techniques to implement memory in extreme conditions. (L2)

**Unit-V:**Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric Random-Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random-Access Memories (MRAMs), Experimental Memory Devices. Memory Hybrids (2D & 3D), Memory Stacks, Memory Testing and Reliability Issues.

**Learning Outcomes:**

1. Examine modern memory technologies with emphasis on future reliability. (L2)

**Text Books:**

1. Ashok K Sharma, "Advanced Semiconductor Memories: Architectures, Designsand Applications", Wiley Interscience
2. KiyooItoh, "VLSI memory chip design", Springer InternationalEdition

**Reference Books:**

1. Ashok K Sharma," Semiconductor Memories: Technology, Testing and Reliability, PHI

**COURSE OUTCOMES VS POs MAPPING (**DETAILED; HIGH:3; MEDIUM:2; LOW:1**):**

| SNO | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 | PSO1 | PSO2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO.1** | 3 | 1 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO.2** | 3 | 1 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO.3** | 3 | 1 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO.4** | 3 | 1 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO.5** | 3 | 1 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO*** | 3 | 1 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |

**** For Entire Course, PO & PSO Mapping***

| Subject Code | Subject Name | Hours | Credits |
|---|---|---|---|
| EC-ESVD1203.2 | SoC Design | 3 | 3 |

**Program Elective-IV**

**Course Objectives:**

Faculty is going to

- List the different ASIC based SoC design methodologies.
- Understand the different no instruction set computer methodology and their development.
- Explain the simulation at different system levels for various constraints.
- Explain the low power SoC design.
- Show the synthesis design of various components and approaches for technology independent and dependent systems.

**Course Outcomes:**

At the end of the course, students will be able to:

1. Illustrate the ASIC based SoC design for various implementations. (L2)
2. Summarize the various methodologies like ASIP, NISC through verification and testing. (L2)
3. Examine the different simulation modes for the design of FPGA based systems. (L3)
4. Discuss the methods of low power design for SoC. (L2)
5. Discuss the technology independent and dependent approaches for synthesis in a SoC design. (L3)

**Unit-I:**

**ASIC:** Overview of ASIC types, design strategies, CISC, RISC and NISC approaches for SOC architectural issues and its impact on SoC design methodologies, Application Specific Instruction Processor (ASIP) concepts.

**Learning Outcomes:**

1. Overview of ASIC types and their functions. (L2)
2. Explain the various architecture issues in the SoC design methodologies. (L2)

**Unit-II:**

**NISC:** NISC Control Words methodology, NISC Applications and Advantages, Architecture Description Languages (ADL) for design and verification of Application Specific Instruction set Processors (ASIP), No-Instruction-Set-computer (NISC)- design flow, modeling NISC architectures and systems, use of Generic Netlist Representation - A formal language for specification, compilation and synthesis of embedded processors.

**Learning Outcomes:**

1. Show the importance of Architecture description language for ASIP. (L2)
2. Summarize the process of formal language specification, compilation, synthesis for embedded processors. (L2)

**Unit-III:**

**Simulation:** Different simulation modes, behavioral, functional, static timing, gate level, switch level, transistor/circuit simulation, design of verification vectors, Low power FPGA, Reconfigurable systems, SoC related modeling of data path design and control logic, Minimization of interconnects impact, clock tree design issues.

**Learning Outcomes:**

1. Show the simulation models for various FPGA based low power design. (L2)
2. Summarize the process of formal language specification, compilation, synthesis for embedded

processors. (L2)

**Unit-IV:Low power SoC design / Digital system:**

Design synergy, Low power system perspective- power gating, clock gating, adaptive voltage scaling (AVS), Static voltage scaling, Dynamic clock frequency and voltage scaling (DCFS), building block optimization, building block memory, power down techniques, power consumption verification.

**Learning Outcomes:**

1. List the methods for low power SoC design. (L2)

**Unit-V:Synthesis**

Role and Concept of graph theory and its relevance to synthesizable constructs, Walks, trails paths, connectivity, components, mapping/visualization, nodal and admittance graph.

Technology independent and technology dependent approaches for synthesis, optimization constraints, Synthesis report analysis Single core and Multi core systems, dark silicon issues, HDL coding techniques for minimization of power consumption, Fault tolerant designs

**Learning Outcomes:**

1. Show the approaches of synthesis with technology independent and dependent characterisitics. (L2)

**Text Books:**


1. Hubert Kaeslin, "Digital Integrated Circuit Design: From VLSI Architectures toCMOS Fabrication", Cambridge University Press,2008.
2. B. Al Hashimi, "System on chip-Next generation electronics", The IET, 2006


**Reference Books:**


1. Rochit Rajsuman, "System-on- a-chip: Design and test", Advantest America R & DCenter,2000
2. P Mishra and N Dutt, "Processor Description Languages", Morgan Kaufmann,2008
3. Michael J. Flynn and Wayne Luk, "Computer System Design: System-on-Chip".Wiley


**COURSE OUTCOMES VS POs MAPPING (**DETAILED; HIGH:3; MEDIUM:2; LOW:1**):**

| SNO | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 | PSO1 | PSO2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO.1** | 3 | 1 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO.2** | 3 | 1 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO.3** | 3 | 1 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO.4** | 3 | 1 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO.5** | 3 | 1 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO*** | 3 | 1 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |

4. **** For Entire Course, PO & PSO Mapping***

| Subject Code | Subject Name | Hours | Credits |
|---|---|---|---|
| EC-ESVD1203.3 | Low Power VLSI Design | 3 | 3 |

**Program Elective-IV**

**Course Objectives:**

Faculty is going to

- List the improvements in technology and circuit level design for low power design.
- Explain the low power circuit techniques for different circuit needs.
- Show the low power clock distribution for simplifying the low power design.
- Logic synthesis for low power estimation techniques.
- Design for low power memory design.

**Course Outcomes:**

At the end of the course, students will be able to:

1. Identify the sources of power dissipation in digital IC systems & understandthe impact of power on system performance andreliability. (L2)
2. Characterize and model power consumption & understand the basic analysis methods. (L2)
3. Summarize the clock distribution and its impact on low power design. (L2)
4. Determine the estimation and synthesis techniques for low power design. (L2)
5. Summarize the low power memory circuits for reduction of power dissipation. (L2)

**Unit-I:** Technology & Circuit Design Levels: Sources of power dissipation in digital ICs, degree Of freedom, recurring themes in low-power, emerging low power approaches, dynamic dissipation in CMOS, effects of Vdd& Vt on speed, constraints on Vt reduction, transistor sizing& optimal gate oxide thickness, impact of technology scaling, technology innovations.

**Learning Outcomes:**

1. List the sources and power dissipation in a digital IC design. (L2)

**Unit-II:**Low Power Circuit Techniques: Power consumption in circuits, flip-flops & latches, high capacitance nodes, energy recovery, reversible pipelines, high performance approaches.

**Learning Outcomes:**

1. Provide low power circuit design techniques for digital circuits. (L2)

**Unit-III:** Low Power Clock Distribution: Power dissipation in clock distribution, single driver Versus distributed buffers, buffers & device sizing under process variations, zero skew Vs. Tolerable skew, chip & package co-design of clock network.

**Learning Outcomes:**

1. Design of clock and distribution to system with a low power consumption. (L2)

**Unit-IV:**Logic Synthesis for Low Power estimation techniques: Power minimization techniques, Low power arithmetic components- circuit design styles, adders, multipliers.

**Learning Outcomes:**

1. Synthesis and estimation techniques for low power design. (L2)

**Unit-V:** Low Power Memory Design: Sources & reduction of power dissipation in memory subsystem, sources of power dissipation in DRAM & SRAM, low power DRAM circuits,
low power SRAM circuits. Low Power Microprocessor Design System: power management support,

architectural trade offs for power, choosing the supply voltage, low-power clocking, implementation problem for low power.

**Learning Outcomes:**

1. Design of low power memory cells and their corresponding memory system design. (L2)

**Text Books:**


1. P. Rashinkar, Paterson and L. Singh, "Low Power Design Methodologies", Kluwer Academic, 2002
2. Kaushik Roy, Sharat Prasad, "Low power CMOS VLSI circuit design", John Wileysons Inc.,2000.


**Reference Books:**


1. J.B.Kulo and J.H Lou, "Low voltage CMOS VLSI Circuits", Wiley,1999.
2. A.P.Chandrasekaran and R.W.Broadersen, "Low power digital CMOSdesign",Kluwer,1995
3. Gary Yeap, "Practical low power digital VLSI design", Kluwer,1998.


**COURSE OUTCOMES VS POs MAPPING (**DETAILED; HIGH:3; MEDIUM:2; LOW:1**):**

| SNO | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 | PSO1 | PSO2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO.1** | 3 | 1 | 1 | 1 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO.2** | 3 | 1 | 1 | 1 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO.3** | 3 | 1 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO.4** | 3 | 1 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO.5** | 3 | 1 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |
| **CO*** | 3 | 1 | 2 | 1 | 2 | - | - | - | - | 2 | - | 2 | 1 | - |

**** For Entire Course, PO & PSO Mapping***

| Subject Code | Subject Name | Hours | Credits |
|---|---|---|---|
| EC-ESVD1204.1 | Communication Busses and Interfaces | 3 | 3 |

**Program Elective -V**

**Course Objectives:**

Faculty is going to

- List the serial busses for device communication.
- Discuss the architecture of standard serial busses.
- Discuss the design and working of USB standard.
- Describe the PCIe as the back end and the preferred bus of communication by the CPU.
- Show the different protocols used in data streaming communication.

**Course Outcomes:**

At the end of the course, students will be able to:

1. Select a particular serial bus suitable for a particularapplication. (L2)
2. Demonstrate the different standard serial architectures in a communication systems. (L3)
3. Develop APIs for configuration, reading and writing data onto serialbus. (L3)
4. Design and develop peripherals that can be interfaced to desired serialbus. (L3)
5. Summarize the data streaming serial communication protocols for enhanced communication systems. (L2)

**UNIT I**

Serial Busses- Cables, Serial busses, serial versus parallel, Data and Control Signal- data frame, data rate, features Limitations and applications of RS232, RS485, $I^2C$ , SPI

**UNIT II CAN**

ARCHITECTURE- ISO 11898-2, ISO 11898-3, Data Transmission- ID allocation, Bit timing, Layers- Application layers, Object layer, Transfer layer, Physical layer, Frame formats- Data frame, Remote frame, Error frame, over load frame, Ack slot, inter frame spacing, Bit spacing, Applications.

**UNIT III PCIe**

Revision, Configuration space- configuration mechanism, Standardized registers, Bus enumeration, Hardware and Software implementation, Hardware protocols, Applications.

**UNIT IV USB**

Transfer Types- Control transfers, Bulk transfer, Interrupt transfer, Isochronous transfer. Enumeration- Device detection, Default state, addressed state, Configured state, enumeration sequencing. Descriptor types and contents- Device descriptor, configuration descriptor, Interface descriptor, Endpoint descriptor, String descriptor. Device driver.

**UNIT V**

Data streaming Serial Communication Protocol- Serial Front Panel Data Port (SFPDP) configurations, Flow control, serial FPDP transmission frames, fiber frames and copper cable.

**TEXTBOOKS**


1. A Comprehensive Guide to controller Area Network – Wilfried Voss, CopperhillMedia Corporation, 2nd Ed., 2005.
2. Serial Port Complete-COM Ports, USB Virtual Com Portsand Ports for Embedded Systems- Jan Axelson, Lakeview Research, 2nd Ed.,


**REFERENCES**


1. USB Complete – Jan Axelson, PenramPublications.
2. PCI Express Technology – Mike Jackson, Ravi Budruk, MindsharePress.

| Subject Code | Subject Name | Hours | Credits |
|---|---|---|---|
| EC-ESVD1204.2 | Network Security andCryptography | 3 | 3 |

**Program Elective -V**

**Course Objectives:**

Faculty is going to

- Explain the theory behind the cryptography.
- Describe the different cryptography techniques.
- Look for authentication and security for a cryptography design.

**Course Outcomes:**

At the end of the course, students will be able to:

- Identify and utilize different forms of cryptographytechniques. (L2)
- Distinguish between symmetric and asymmetric cryptography design. (L4)
- Summarize the cryptography in a private and public key systems. (L2)
- Incorporate authentication and security in the networkapplications. (L3)
- Distinguish among different types of threats to the system and handle thesame. (L4)

**Unit-I:Security & Number Theory**

Need, security services, Attacks, OSI Security Architecture, one time passwords, Model for Network security, Classical Encryption Techniques like substitution ciphers, Transposition ciphers, Cryptanalysis of Classical Encryption Techniques. Introduction, Fermat‟s and Euler‟s Theorem, The Chinese Remainder Theorem, Euclidean Algorithm, Extended Euclidean Algorithm, and Modular Arithmetic.

**Unit-II: Private-Key (Symmetric) Cryptography**

Block Ciphers, Stream Ciphers, RC4 Stream cipher, Data Encryption Standard (DES),Advanced Encryption Standard (AES), Triple DES, RC5, IDEA, Linear and Differential Cryptanalysis.

**Unit-III:Public-Key (Asymmetric) Cryptography**

RSA, Key Distribution and Management, Diffie-Hellman Key Exchange, Elliptic Curve Cryptography, Message Authentication Code, hash functions, message digest algorithms: MD4 MD5, Secure Hash algorithm, RIPEMD-160, HMAC.

**Unit-IV:Authentication**

IP and Web Security Digital Signatures, Digital Signature Standards, Authentication Protocols, Kerberos, IP security Architecture, Encapsulating Security Payload, Key Management, Web Security Considerations, Secure Socket Layer and Transport Layer Security, Secure Electronic Transaction.

**Unit-V:System Security**

Intruders, Intrusion Detection, Password Management, Worms, viruses, Trojans, Virus Countermeasures, Firewalls, Firewall Design Principles, Trusted Systems.

**Text Books:**


1. William Stallings, “Cryptography and Network Security, Principles and Practices”,Pearson Education, 3rdEdition.
2. Charlie Kaufman, Radia Perlman and Mike Speciner, “Network Security, Private Communication in a Public World”, Prentice Hall, 2nd Edition


**Reference Books:**


1. Christopher M. King, Ertem Osmanoglu, Curtis Dalton, “Security Architecture,Design Deployment and Operations”, RSAPres,
2. Stephen Northcutt, LenyZeltser, Scott Winters, Karen Kent, and Ronald W. Ritchey, “Inside Network Perimeter Security”, Pearson Education, 2ndEdition
3. Richard Bejtlich, “The Practice of Network Security Monitoring: UnderstandingIncident Detection and Response”, William Pollock Publisher,2013.

| Subject Code | Subject Name | Hours | Credits |
|---|---|---|---|
| EC-ESVD1204.3 | Physical Design Automation | 3 | 3 |

**Program Elective -V**

**Course Objectives:**

Faculty is going to

- List the design cycle and the rules for physical design.
- List the factors effecting the physical stability of a system.
- Show the portioning and graphing algorithms for the physical design.

**Course Outcomes:**

At the end of the course, students will be able to:

1. Understand the relationship between design automation algorithms and Various constraints posed by VLSI fabrication and designtechnology. (L2)
2. Adapt the design algorithms to meet the critical designparameters. (L3)
3. List the data structures and algorithms needed for design automation. (L2)
4. Identify layout optimization techniques and map them to thealgorithms. (L2)
5. Develop proto-type EDA tool and test itsefficacy. (L3)

**UNIT -I**

VLSI design Cycle, Physical Design Cycle, Design Rules, Layout of Basic Devices, and Additional Fabrication, Design styles: full custom, standard cell, gate arrays, field programmable gate arrays, sea of gates and comparison, system packaging styles, multi-chip modules. Design rules, layout of basic devices, fabrication process and its impact on physical design, interconnect delay, noise and cross talk, yield and fabrication cost.

**UNIT -II:**

Factors, Complexity Issues and NP-hard Problems, Basic Algorithms (Graph and Computational Geometry): graph search algorithms, spanning tree algorithms, shortest path algorithms, matching algorithms, min-cut and max-cut algorithms, Steiner tree algorithms

**UNIT -III:**

Basic Data Structures, atomic operations for layout editors, linked list of blocks, bin based methods, neighbour pointers, corner stitching, multi-layer operations.

**UNIT -IV:**

Graph algorithms for physical design: classes of graphs, graphs related to a set of lines, graphs related to set of rectangles, graph problems in physical design, maximum clique and minimum colouring, maximum k-independent set algorithm, algorithms for circlegraphs.

**UNIT -V:**

Partitioning algorithms: design style specific partitioning problems, group migrated algorithms, simulated annealing and evolution, and Floor planning and pin assignment, Routing and placement algorithms

**Text Books:**


1. Naveed Shervani, Algorithms for VLSI Physical Design Automation, 3rd Edition, Kluwer Academic,1999.
2. Charles J Alpert, Dinesh P Mehta, Sachin S Sapatnekar, Handbook of Algorithms for Physical Design Automation, CRC Press,2008

| Subject Code | Subject Name | Hours | Credits |
|---|---|---|---|
| EC-ESVD1205.1 | BUSSINESS ANALYTICS | 3 | 3 |

**(Open Elective)**

**Course Outcomes:**

1. Students will demonstrate knowledge of data analytics.
2. Students will demonstrate the ability of think critically in making decisions based on data and deep analytics.
3. Students will demonstrate the ability to use technical skills in predicative and prescriptive modeling to support business decision-making.
4. Students will demonstrate the ability to translate data into clear, actionable insights

**Unit-I:**

**Business analytics**: Overview of Business analytics, Scope of Business analytics, Business Analytics Process, Relationship of Business Analytics Process and organisation, competitive advantages of Business Analytics.

**Statistical Tools:** Statistical Notation, Descriptive Statistical methods,

Review of probability distribution and data modelling, sampling and estimation methods overview.

**Unit-II:**

**Trendiness and Regression Analysis:** Modelling Relationships and Trends in Data, simple Linear Regression.Important Resources, Business Analytics Personnel, Data and modelsfor Business analytics, problem solving, Visualizing and Exploring Data, Business Analytics Technology

**Unit-III:**

Organization Structures of Business analytics, Team management, Management Issues, Designing Information Policy, Outsourcing, Ensuring Data Quality, Measuring contribution of Business analytics, Managing Changes.Descriptive Analytics, predictive analytics, predicative Modelling, Predictive analytics analysis,DataMining,Data Mining Methodologies, Prescriptive analytics and its step in the business analytics Process, Prescriptive Modelling, nonlinear Optimization.

**Unit-IV:**

**Forecasting Techniques:** Qualitative and Judgmental Forecasting, Statistical Forecasting Models, Forecasting Models for Stationary Time Series, Forecasting Models for Time Series with a Linear Trend, Forecasting Time Series with Seasonality, Regression Forecasting with Casual Variables, Selecting Appropriate Forecasting Models.

Monte Carlo Simulation and Risk Analysis: Monte CarleSimulation

Using Analytic Solver Platform, New-Product Development Model, Newsvendor Model, Overbooking Model, Cash Budget Model.

**Unit-V:**

**Decision Analysis:** Formulating Decision Problems, Decision Strategies with the without Outcome Probabilities, Decision Trees, The Value of Information, Utility and Decision Making.

Recent Trends in : Embedded and collaborative business intelligence,Visual data recovery, Data Storytelling and Data journalism

**Reference:**


1. Business analytics Principles, Concepts, and Applications by Marc J. Schniederjans, Dara G. Schniederjans, Christopher M. Starkey, Pearson FTPress.
2. Business Analytics by James Evans, personsEducation.

| Subject Code | Subject Name | Hours | Credits |
|---|---|---|---|
| EC-ESVD1205.2 | INDUSTRIAL SAFETY | 3 | 3 |

**(Open Elective)**

**Unit-I:**

Industrial safety: Accident, causes, types, results and control, mechanical and electrical hazards, types, causes and preventive steps/procedure, describe salient points of factories act 1948 for health and safety, wash rooms, drinking water layouts, light, cleanliness, fire, guarding, pressure vessels, etc, Safety color codes. Fire prevention and firefighting, equipment and methods.

**Unit-II:**

Fundamentals of maintenance engineering: Definition and aim of maintenance engineering, Primary and secondary functions and responsibility of maintenance department, Types of maintenance, Types and applications of tools used for maintenance, Maintenance cost & its relation with replacement economy, Service life of equipment.

**Unit-III:**

Wear and Corrosion and their prevention: Wear- types, causes, effects, wear reduction methods, lubricants-types and applications, Lubrication methods, general sketch, working and applications, i. Screw down grease cup, ii. Pressure grease gun, iii. Splash lubrication, iv. Gravity lubrication, v. Wick feed lubrication vi. Side feed lubrication, vii. Ring lubrication, Definition, principle and factors affecting the corrosion. Types of corrosion, corrosion prevention methods.

**Unit-IV:**

Fault tracing: Fault tracing-concept and importance, decision tree concept, need and applications, sequence of fault finding activities, show as decision tree, draw decision tree for problems in machine tools, hydraulic, pneumatic, automotive, thermal and electrical equipment‟s like, I. Any one machine tool, ii. Pump iii. Air compressor, iv. Internal combustion engine,v. Boiler,vi .Electrical motors, Types of faults in machine tools and their general causes.

**Unit-V:**

Periodic and preventive maintenance: Periodic inspection-concept and need, degreasing, cleaning and repairing schemes, overhauling of mechanical components, overhauling of electrical motor, common troubles and remedies of electric motor, repair complexities and its use, definition, need, steps and advantages of preventive maintenance. Steps/procedure for periodic and preventive maintenance of: I. Machine tools, ii. Pumps, iii.Air compressors, iv. Diesel generating (DG) sets, Program and schedule of preventive maintenance of mechanical and electrical equipment, advantages of preventive maintenance. Repair cycle concept and importance

**References:**


1. Maintenance Engineering Handbook, Higgins & Morrow, Da InformationServices.
2. Maintenance Engineering, H. P. Garg, S. Chand andCompany.
3. Pump-hydraulic Compressors, Audels, McgrewHillPublication.
4. Foundation Engineering Handbook, Winterkorn, Hans, Chapman &HallLondon

| Subject Code | Subject Name | Hours | Credits |
|---|---|---|---|
| EC-ESVD1205.3 | OPERATIONS RESEARCH | 3 | 3 |

**(Open Elective)**

**Course Outcomes:**

At the end of the course, the student should be able to

1. Students should able to apply the dynamic programming to solve problems of discreet and continuous variables.
2. Students should able to apply the concept of non-linear programming
3. Students should able to carry out sensitivity analysis
4. Student should able to model the real world problem and simulate it.

**Unit-I**:

Optimization Techniques, Model Formulation, models, General L.R Formulation, Simplex Techniques, Sensitivity Analysis, Inventory Control Models

**Unit-II**

Formulation of a LPP - Graphical solution revised simplex method - duality theory - dual simplex method - sensitivity analysis - parametric programming

**Unit-III**:

Nonlinear programming problem - Kuhn-Tucker conditions min cost flow problem - max flow problem - CPM/PERT

**Unit-IV**

Scheduling and sequencing - single server and multiple server models - deterministic inventory models - Probabilistic inventory control models - Geometric Programming.

**Unit-V**

Competitive Models, Single and Multi-channel Problems, Sequencing Models, Dynamic Programming, Flow in Networks, Elementary Graph Theory, Game Theory Simulation

**References**:


1. H.A. Taha, Operations Research, An Introduction, PHI, 2008
2. H.M. Wagner, Principles of Operations Research, PHI, Delhi, 1982.
3. J.C. Pant, Introduction to Optimisation: Operations Research, Jain Brothers, Delhi, 2008
4. Hitler Libermann Operations Research: McGraw Hill Pub. 2009
5. Pannerselvam, Operations Research: Prentice Hall of India 2010
6. Harvey M Wagner, Principles of Operations Research: Prentice Hall of India 2010

| Subject Code | Subject Name | Hours | Credits |
|---|---|---|---|
| EC-ESVD1205.4 | COST MANAGEMENT OF ENGINEERING PROJECTS | 3 | 3 |

**(Open Elective)**

**Unit-I**:
Introduction and Overview of the Strategic Cost Management Process

**Unit-II**:
Cost concepts in decision-making; Relevant cost, Differential cost, Incremental cost and Opportunity cost. Objectives of a Costing System; Inventory valuation; Creation of a Database for operational control; Provision of data for Decision-Making.

**Unit-III**:
Project: meaning, Different types, why to manage, cost overruns centres, various stages of project execution: conception to commissioning. Project execution as conglomeration of technical and non- technical activities. Detailed Engineering activities. Pre project execution main clearances and documents Project team: Role of each member. Importance Project site: Data required with significance. Project contracts. Types and contents. Project execution Project cost control. Bar charts and Network diagram. Project commissioning: mechanical and process

**Unit-IV**:
Cost Behavior and Profit Planning Marginal Costing; Distinction between Marginal Costing and Absorption Costing; Break-even Analysis, Cost-Volume-Profit Analysis. Various decision-making problems. Standard costing and Variance Analysis. Pricing strategies: Pareto Analysis. Target costing, Life Cycle Costing. Costing of service sector. Just-in-time approach, Material Requirement Planning, Enterprise Resource Planning,

**Unit-V**:
Total Quality Management and Theory of constraints. Activity-Based Cost Management, Bench Marking; Balanced Score Card and Value-Chain Analysis. Budgetary Control; Flexible Budgets; Performance budgets; Zero-based budgets. Measurement of Divisional profitability pricing decisions including transfer pricing.
Quantitative techniques for cost management, Linear Programming, PERT/CPM, Transportation problems, Assignment problems, Simulation, Learning Curve Theory.

**References:**


1. Cost Accounting A Managerial Emphasis, Prentice Hall of India, New Delhi
2. Charles T. Horngren and George Foster, Advanced Management Accounting
3. Robert S Kaplan Anthony A. Alkinson, Management & Cost Accounting
4. Ashish K. Bhattacharya, Principles & Practices of Cost Accounting A. H. Wheeler publisher
5. N.D. Vohra, Quantitative Techniques in Management, Tata McGraw Hill Book Co. Ltd.

| Subject Code | Subject Name | Hours | Credits |
|---|---|---|---|
| EC-ESVD1205.5 | COMPOSITE MATERIALS | 3 | 3 |

**(Open Elective)**

**UNIT–I**:

INTRODUCTION: Definition – Classification and characteristics of Composite materials. Advantages and application of composites. Functional requirements of reinforcement and matrix.Effect of reinforcement (size, shape, distribution, volume fraction) on overall composite performance.

**UNIT – II**:

REINFORCEMENTS: Preparation-layup, curing, properties and applications of glass fibers, carbon fibers, Kevlar fibers and Boron fibers. Properties and applications of whiskers, particle reinforcements. Mechanical Behavior of composites: Rule of mixtures, Inverse rule of mixtures. Isostrain and Isostress conditions.

**UNIT – III:**

Manufacturing of Metal Matrix Composites: Casting – Solid State diffusion technique, Cladding – Hot isostaticpressing. Properties and applications. Manufacturing of Ceramic Matrix Composites: Liquid Metal Infiltration – Liquid phase sintering. Manufacturing of Carbon – Carbon composites: Knitting, Braiding, Weaving. Properties and applications.

**UNIT–IV:**

Manufacturing of Polymer Matrix Composites: Preparation of Moulding compounds and prepregs – hand layup method – Autoclave method – Filament winding method – Compression moulding – Reaction injection moulding. Properties and applications.

**UNIT – V:**

Strength: Laminar Failure Criteria-strength ratio, maximum stress criteria, maximum strain criteria, interacting failure criteria, hygrothermal failure. Laminate first play failure-insight strength; Laminate strength-ply discount truncated maximum strain criterion; strength design using caplet plots; stress concentrations.

**TEXT BOOKS:**


1. Material Science and Technology – Vol 13 – Composites by R.W.Cahn – VCH, West Germany.
2. Materials Science and Engineering, An introduction. WD Callister, Jr., Adapted by R. Balasubramaniam, John Wiley & Sons, NY, Indian edition,2007.


**References:**


1. Hand Book of CompositeMaterials-ed-Lubin.
2. Composite Materials – K.K.Chawla.
3. Composite Materials Science and Applications – Deborah D.L.Chung.
4. Composite Materials Design and Applications – Danial Gay, Suong V. Hoa, and Stephen W. Tasi.

| Subject Code | Subject Name | Hours | Credits |
|---|---|---|---|
| EC-ESVD1205.6 | WASTE OF ENERGY | 3 | 3 |

**(Open Elective)**

**Unit-I:**

Introduction to Energy from Waste: Classification of waste as fuel – Agro based, Forest residue, Industrial waste - MSW – Conversion devices – Incinerators, gasifiers, digestors

**Unit-II:**

Biomass Pyrolysis: Pyrolysis – Types, slow fast – Manufacture of charcoal – Methods - Yields and application – Manufacture of pyrolytic oils and gases, yields and applications.

**Unit-III:**

Biomass Gasification: Gasifiers – Fixed bed system – Downdraft and updraft gasifiers – Fluidized bed gasifiers – Design, construction and operation – Gasifier burner arrangement for
thermal heating – Gasifier engine arrangement and electrical power – Equilibrium and kinetic consideration in gasifier operation

**Unit-IV:**

Biomass Combustion: Biomass stoves – Improved chullahs, types, some exotic designs, Fixed bed combustors, Types, inclined grate combustors, Fluidized bed combustors, Design, construction and operation - Operation of all the above biomass combustors.

**Unit-V:**

Biogas: Properties of biogas (Calorific value and composition) - Biogas plant technology and status - Bio energy system - Design and constructional features - Biomass resources and their classification - Biomass conversion processes - Thermo chemical conversion - Direct combustion - biomass gasification
- pyrolysis and liquefaction - biochemical conversion - anaerobic digestion - Types of biogas Plants – Applications - Alcohol production from biomass - Bio diesel production - Urban waste to energy conversion - Biomass energy programme in India.

**References:**


1. Non Conventional Energy, Desai, Ashok V., Wiley Eastern Ltd., 1990.
2. Biogas Technology - A Practical Hand Book - Khandelwal, K. C. and Mahdi, S. S., Vol. I & II, Tata McGraw Hill Publishing Co. Ltd., 1983.
3. Food, Feed and Fuel from Biomass, Challal, D. S., IBH Publishing Co. Pvt. Ltd., 1991.
4. Biomass Conversion and Technology, C. Y. WereKo-Brobby and E. B. Hagan, John Wiley & Sons, 1996.

| Subject Code | Subject Name | Hours | Credits |
|---|---|---|---|
| **EC-ESVD1206** | **Analog and Digital CMOS VLSI Design Lab** | **4** | **2** |

The students are required to design and implement the Circuit and Layout of any **TEN** Experiments using CMOS 130nm Technology with Mentor Graphics Tool/Cadence/ Synopsys/Industry Equivalent StandardSoftware.

**List of Experiments:**

1. MOS Device Characterization and parametricanalysis
2. Common SourceAmplifier
3. Common Source Amplifier with sourcedegeneration
4. Cascodeamplifier
5. simple currentmirror
6. cascode current mirror.
7. Wilson currentmirror.
8. FullAdder
9. RS-Latch
10. ClockDivider
11. JK-FlipFlop
12. SynchronousCounter
13. AsynchronousCounter
14. Static RAMCell

| Subject Code | Subject Name | Hours | Credits |
|---|---|---|---|
| EC-ESVD1207 | Real Time Operating Systems Lab | 4 | 2 |

- The Students are required to write the programs using C-Language according to theExperiment requirements using RTOS Library Functions and macros ARM-926 developer kits and ARM-Cortex.
- The following experiments are required to develop the algorithms, flow diagrams, source code and perform the compilation, execution and implement the same using necessary hardwarekits for verification. The programs developed for the implementation should be at the level of an embedded systemdesign.
- The students are required to perform at least SIX experiments from Part-I and TWO experiments fromPart-II.

**List of Experiments:**

**Part-I:Experiments using ARM-926 with PERFECT RTOS**

1. Register a new command inCLI.
2. Create a newTask.
3. Interrupthandling.
4. Allocate resource usingsemaphores.
5. Share resource usingMUTEX.
6. Avoid deadlock using BANKER"Salgorithm.
7. Synchronize two identical threads usingMONITOR.
8. Reader"s Writer"s Problem for concurrentTasks.

**Part-II: Experiments on ARM-CORTEX processor using any open source RTOS. (Coo-Cox-Software-Platform)**

1. Implement the interfacing of display with the ARM- CORTEXprocessor.
2. Interface ADC and DAC ports with the Input and Output sensitivedevices.
3. Simulate the temperature DATA Logger with the SERIALcommunication with PC.
4. Implement the developer board as a modem for data communicationusing serial port communication between twoPC"s.

**Lab Requirements:**

**Software:**

- Eclipse IDE for C and C++ (YAGARTO Eclipse IDE), Perfect RTOSLibrary, COO-COX Software Platform, YAGARTO TOOLS, and TFTPSERVER.
- LINUX Environment for the compilation using Eclipse IDE & Java withlatest version.

**Hardware:**

- The development kits of ARM-926 Developer Kits and ARM-CortexBoards.
- Serial Cables, Network Cables and recommended power supply for theboard.

| Subject Code | Subject Name | Hours | Credits |
|---|---|---|---|
| EC-ESVD1208 | Mini project | 4 | 2 |

**MINI PROJECT**

**Syllabus Contents**

The students are required to search / gather the material / information on a specific a topic comprehend it and present / discuss in the class.

**Course Outcomes**

At the end of this course, students will be able to

1. Understand of contemporary / emerging technology for various processes and systems.
2. Share knowledge effectively in oral and written form and formulatedocuments

## AUDIT 1 and 2: ENGLISH FOR RESEARCH PAPER WRITING

**Course objectives:**

Students will be able to:

Understand that how to improve your writing skills and level of readability Learn about what to write in each section

Understand the skills needed when writing a Title Ensure the good quality of paper at very first-time submission

**Syllabus**

| Units | CONTENTS |
|---|---|
| 1 | Planning and Preparation, Word Order, Breaking up long sentences,Structuring Paragraphs and Sentences, Being Conciseand Removing Redundancy, Avoiding Ambiguity and Vagueness |
| 2 | Clarifying Who Did What, Highlighting Your Findings, Hedgingand Criticising, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts. Introduction |
| 3 | Review of the Literature, Methods, Results, Discussion,Conclusions, The Final Check. |
| 4 | key skills are needed when writing a Title, key skills are neededwhen writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature, |
| 5 | skills are needed when writing the Methods, skills needed whenwriting the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions |
| 6 | useful phrases, how to ensure paper is as good as it could possibly be the first- time submission |

**Text Books:**


1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books)
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press
3. HighmanN(1998),HandbookofWritingfortheMathematicalSciences,SIAM. Highman'sbook .
4. Adrian Wallwork , English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011

## AUDIT 1 and 2: DISASTER MANAGEMENT

**Course Objectives: -**Students will be able to:

- learn to demonstrate a critical understanding of key concepts in disaster risk reduction and humanitarian response.
- critically evaluate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
- develop an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
- critically understand the strengths and weaknesses of disaster management approaches, planning and programming in different countries, particularly their home country or the countriesthey work in

**Syllabus**

| Units | CONTENTS |
|---|---|
| 1 | **Introduction**<br>Disaster: Definition, Factors And Significance; Difference Between Hazard And Disaster; Natural And Manmade Disasters: Difference, Nature, Types And Magnitude. |
| 2 | **Repercussions Of Disasters And Hazards**: Economic Damage, Loss Of Human And Animal Life, Destruction Of Ecosystem.<br>Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts And Famines, Landslides And Avalanches, Man- made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks And Spills, Outbreaks Of Disease And Epidemics, War AndConflicts. |
| 3 | **Disaster Prone Areas In India**<br>Study Of Seismic Zones; Areas Prone To Floods And Droughts, Landslides And Avalanches; Areas Prone To Cyclonic And Coastal Hazards With Special Reference To Tsunami; Post-Disaster DiseasesAnd Epidemics |
| 4 | **Disaster Preparedness And Management**<br>Preparedness: Monitoring Of Phenomena Triggering A Disaster Or Hazard; Evaluation Of Risk: Application Of Remote Sensing, DataFrom Meteorological And Other Agencies, Media Reports: Governmental And Community Preparedness. |
| 5 | **Risk Assessment**<br>Disaster Risk: Concept And Elements, Disaster Risk Reduction, Global And National Disaster Risk Situation. Techniques Of Risk Assessment,Global Co-Operation In Risk Assessment And Warning, People‟s Participation In Risk Assessment. Strategies for Survival. |
| 6 | **Disaster Mitigation**<br>Meaning, Concept And Strategies Of Disaster Mitigation, Emerging TrendsInMitigation.Structural MitigationAndNon-StructuralMitigation, Programs Of Disaster Mitigation In India. |

**Text Books:**


1. R. Nishith, Singh AK, “Disaster Management in India: Perspectives, issues and strategies ““New Royal book Company.
2. Sahni, PardeepEt.Al. (Eds.),” Disaster Mitigation Experiences And Reflections”, Prentice Hall Of India, New Delhi.
3. Goel S. L. , Disaster Administration And Management Text And Case Studies” ,Deep &Deep Publication Pvt. Ltd., New Delhi.

## AUDIT 1 and 2: SANSKRIT FOR TECHNICAL KNOWLEDGE

**Course Objectives**

- To get a working knowledge in illustrious Sanskrit, the scientific language in the world
- Learning of Sanskrit to improve brain functioning
- Learning of Sanskrit to develop the logic in mathematics, science & other subjects enhancing the memory power
- The engineering scholars equipped with Sanskrit will be able to explore the huge knowledge from ancient literature

**Course Outcome**

Students will be able to

1. Understanding basic Sanskrit language
2. Ancient Sanskrit literature about science & technology can be understood
3. Being a logical language will help to develop logic in students

**Syllabus**

| Unit | Content |
|---|---|
| 1 | • Alphabets in Sanskrit,<br>• Past/Present/Future Tense,<br>• Simple Sentences |
| 2 | • Order<br>• Introduction of roots<br>• Technical information about Sanskrit Literature |
| 3 | • Technical concepts of Engineering-Electrical, Mechanical, Architecture,Mathematics |

**Text Books:**


1. "Abhyaspustakam" – Dr.Vishwas, Samskrita-Bharti Publication, New Delhi
2. "Teach Yourself Sanskrit" Prathama Deeksha-Vempati Kutumbshastri, Rashtriya Sanskrit Sansthanam, New Delhi Publication
3. "India‟s Glorious Scientific Tradition" Suresh Soni, Ocean books (P) Ltd., New Delhi.

## AUDIT 1 and 2: VALUE EDUCATION

**Course Objectives**

Students will be able to

- Understand value of education and self- development
- Imbibe good values in students
- Let the should know about the importance of character

**Course outcomes**

Students will be able to

1. Knowledge of self-development
2. Learn the importance of Human values
3. Developing the overall personality

**Syllabus**

| Unit | Content |
|---|---|
| 1 | Values and self-development –Social values and individual attitudes. Work ethics, Indian vision of humanism.<br>Moral and non- moral valuation. Standards and principles.<br>Value judgements |
| 2 | Importance of cultivation of values.<br>Sense of duty. Devotion, Self-reliance. Confidence, Concentration. Truthfulness, Cleanliness.<br>Honesty, Humanity. Power of faith, National Unity.<br>Patriotism.Love for nature,Discipline |
| 3 | Personality and Behavior Development - Soul and Scientific attitude. Positive Thinking. Integrity and discipline.<br>Punctuality, Love and Kindness.<br>Avoid fault Thinking.<br>Free from anger, Dignity of labor.<br>Universal brotherhood and religious tolerance.<br>True friendship.<br>Happiness Vs suffering, love for truth.<br>Aware of self-destructive habits.<br>Association and Cooperation.<br>Doing best for saving nature |
| 4 | Character and Competence –Holy books vs Blind faith.<br>Self-management and good health.<br>Science of reincarnation.<br>Equality, Nonviolence,Humility, Role of Women.<br>All religions and same message.<br>Mind your Mind, Self-control.<br>Honesty, Studying effectively |

**Text Books:**

1 Chakroborty, S.K. “Values and Ethics for organizations Theory and practice”, Oxford University Press, New Delhi

## AUDIT 1 and 2: CONSTITUTION OF INDIA

**Course Objectives:**

Students will be able to:

- Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective.
- To address the growth of Indian opinion regarding modern Indian intellectuals‟ constitutional role and entitlement to civil and economic rights as well as the emergence of nationhood in the early years of Indian nationalism.
- To address the role of socialism in India after the commencement of the Bolshevik Revolution in 1917 and its impact on the initial drafting of the Indian Constitution.

**Course Outcomes:**

Students will be able to:

1. Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.
2. Discuss theintellectualorigins ofthe frameworkof argument that informedtheconceptualization of social reforms leading to revolution in India.
3. Discuss the circumstances surrounding the foundation of the Congress Socialist Party [CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.
4. Discuss the passage of the Hindu Code Bill of 1956.

| **Syllabus** | |
|---|---|
| **Units** | **Content** |
| **1** | **History of Making of the Indian Constitution:**<br>History<br>Drafting Committee, ( Composition & Working) |
| **2** | **Philosophy of the Indian Constitution:**<br>Preamble Salient Features |
| **3** | **Contours of Constitutional Rights & Duties:**<br>Fundamental Rights Right to Equality Right to Freedom<br>Right against Exploitation Right to Freedom of Religion Cultural and Educational Rights<br>Right to Constitutional Remedies Directive Principles of State Policy Fundamental Duties. |
| **4** | **Organs of Governance:** Parliament Composition<br>Qualifications and Disqualifications Powers and Functions<br>Executive President Governor<br>Council of Ministers<br>Judiciary, Appointment and Transfer of Judges, Qualifications Powers and Functions |
| **5** | **Local Administration:**<br>District‟s Administration head: Role and Importance,<br>Municipalities: Introduction, Mayor and role of Elected Representative, CE of Municipal Corporation.<br>Pachayati raj: Introduction, PRI: ZilaPachayat.<br>Elected officials and their roles, CEO ZilaPachayat: Position and role. Block level: |

| | |
|---|---|
| | Organizational Hierarchy (Different departments), Village level: Role of Elected and Appointed officials,<br>Importance of grass root democracy |
| **6** | **Election Commission:**<br>Election Commission: Role and Functioning.<br>Chief Election Commissioner and Election Commissioners. State Election Commission: Role and Functioning.<br>Institute and Bodies for the welfare of SC/ST/OBC and women. |

**Text Books:**


1. The Constitution of India, 1950 (Bare Act), Government Publication.
2. Dr. S. N. Busi, Dr. B. R. Ambedkar framing of Indian Constitution, 1st Edition, 2015.
3. M. P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis, 2014.
4. D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 2015.

## AUDIT 1 and 2: PEDAGOGY STUDIES

**Course Objectives:**

Students will be able to:

1. Review existing evidence on the review topic to inform programme design and policy making undertaken by the DfID, other agencies and researchers.
2. Identify critical evidence gaps to guide the development.

**Course Outcomes:**

Students will be able to understand:

1. What pedagogical practices are being used by teachers in formal and informal classrooms in developing countries?
2. What is the evidence on the effectiveness of these pedagogical practices, in what conditions, and with what population of learners?
3. How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy?

| Units | Content |
|---|---|
| 1 | **Introduction and Methodology:**<br>• Aims and rationale, Policy background, Conceptual framework and terminology<br>• Theories of learning, Curriculum, Teacher education.<br>• Conceptual framework, Research questions**.**<br>• Overview of methodology and Searching. |
| 2 | • Thematic overview: Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries.<br>• Curriculum, Teacher education. |
| 3 | • Evidence on the effectiveness of pedagogical practices<br>• Methodology for the in depth stage: quality assessment of included studies.<br>• How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy?<br>• Theory of change.<br>• Strength and nature of the body of evidence for effective pedagogical practices.<br>• Pedagogic theory and pedagogical approaches.<br>• Teachers‟ attitudes and beliefs and Pedagogic strategies. |
| 4 | • Professional development: alignment with classroom practices and follow-up support<br>• Peer support<br>• Support from the head teacher and the community.<br>• Curriculum and assessment<br>• Barriers to learning: limited resources and large class sizes |
| 5 | **Research gaps and future directions**<br>• Research design<br>• Contexts<br>• Pedagogy<br>• Teacher education<br>• Curriculum and assessment<br>• Dissemination and research impact. |

**Text Books:**


1. Ackers J, Hardman F (2001) Classroom interaction in Kenyan primary schools, Compare, 31 (2): 245-261.
2. Agrawal M (2004) Curricular reform in schools: The importance of evaluation, Journal of Curriculum Studies, 36 (3): 361-379.
3. Akyeampong K (2003) Teacher training in Ghana - does it count? Multi-site teacher education research project (MUSTER) country report 1. London: DFID.
4. Akyeampong K, Lussier K, Pryor J, Westbrook J (2013) Improving teaching and learning of basic maths and reading in Africa: Does teacher preparation count? International Journal Educational Development, 33 (3): 272–282.
5. Alexander RJ (2001) Culture and pedagogy: International comparisons in primary education. Oxford and Boston: Blackwell.
6. Chavan M (2003) Read India: A mass scale, rapid, „learning to read" campaign.
7. www.pratham.org/images/resource%20working%20paper%202.pdf.

## AUDIT 1 and 2: STRESS MANAGEMENT BY YOGA

**Course Objectives**

1. To achieve overall health of body and mind
2. To overcome stress

**Course Outcomes:**

Students will be able to:

1. Develop healthy mind in a healthy body thus improving social health also
2. Improve efficiency

**Syllabus**

| Unit | Content |
|---|---|
| 1 | • Definitions of Eight parts of yog. ( Ashtanga ) |
| 2 | Yam and Niyam. Do`s and Don‟t‟s in life.<br>i) Ahinsa, satya, astheya, bramhacharya and aparigraha<br>ii) Shaucha, santosh, tapa, swadhyay, ishwarpranidhan |
| 3 | Asan and Pranayam<br>1. Various yog poses and their benefits for mind & body<br>2. Regularization of breathing techniques and its effects-Types of pranayam |

**Text Books:**


1. „Yogic Asanas for Group Tarining-Part-I” : Janardan Swami YogabhyasiMandal, Nagpur
2. “Rajayoga or conquering the Internal Nature” by Swami Vivekananda, Advaita Ashrama (Publication Department), Kolkata

**AUDIT 1 and 2: PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTENMENT SKILLS**

**Course Objectives**

1. To learn to achieve the highest goal happily
2. To become a person with stable mind, pleasing personality and determination
3. To awaken wisdom in students

**Course Outcomes**

Students will be able to

1. Study of Shrimad-Bhagwad-Geeta will help the student in developing his personality and achieve the highest goal in life
2. The person who has studied Geeta will lead the nation and mankind to peace and prosperity
3. Study of Neetishatakam will help in developing versatile personality of students

**Syllabus**

| Unit | Content |
|---|---|
| 1 | Neetisatakam-Holistic development of personality<br>• Verses- 19,20,21,22 (wisdom)<br>• Verses- 29,31,32 (pride & heroism)<br>• Verses- 26,28,63,65 (virtue)<br>• Verses- 52,53,59 (dont‟s)<br>• Verses- 71,73,75,78 (do‟s) |
| 2 | • Approach to day to day work and duties.<br>• Shrimad Bhagwad Geeta : Chapter 2-Verses 41, 47,48,<br>• Chapter 3-Verses 13, 21, 27, 35, Chapter 6-Verses 5,13,17, 23, 35,<br>• Chapter 18-Verses 45, 46, 48. |
| 3 | • Statements of basic knowledge.<br>• Shrimad Bhagwad Geeta: Chapter2-Verses 56, 62, 68<br>• Chapter 12 -Verses 13, 14, 15, 16,17, 18<br>• Personality of Role model. Shrimad Bhagwad Geeta: Chapter2- Verses 17, Chapter 3-Verses 36,37,42,<br>• Chapter 4-Verses 18, 38,39<br>• Chapter18 – Verses 37,38,63 |

**Text Books:**

1. “Srimad Bhagavad Gita” by Swami Swarupananda Advaita Ashram (Publication Department), Kolkata
2. Bhartrihari‟s Three Satakam (Niti-sringar-vairagya) by P.Gopinath, Rashtriya Sanskrit Sansthanam, New Delhi.

## (DISSERTATION) DISSERTATION PHASE – I AND PHASE – II

**Course Outcomes:**

At the end of this course, students will be able to

1. Ability to synthesize knowledge and skills previously gained and applied to an in-depth study and execution of new technicalproblem.
2. Capable to select from different methodologies, methods and forms of analysis to produce a suitable research design, and justify theirdesign.
3. Ability to present the findings of their technical solution in a writtenreport.
4. Presenting the work in International/ National conference or reputedjournals.

**Syllabus Contents:**

The dissertation / project topic should be selected / chosen to ensure the satisfaction of the urgent need to establish a direct link between education, national development and productivity and thus reduce the gap between the world of work and the world of study. The dissertation should have the following

- Relevance to social needs ofsociety
- Relevance to value addition to existing facilities in theinstitute
- Relevance to industry need
- Problems of national importance

Research and development in various domain The student should complete thefollowing:

- Literature survey ProblemDefinition
- Motivation for study andObjectives
- Preliminary design / feasibility / modularapproaches
- Implementation and Verification
- Report andpresentation

The dissertation stage II is based on a report prepared by the students on dissertation allotted to them. It may be based on:

- Experimental verification / Proof ofconcept.
- Design, fabrication, testing of CommunicationSystem.
- The viva-voce examination will be based on the above report andwork.

**Guidelines for Dissertation Phase – I and II at M. Tech. (Electronics):**

- As per the AICTE directives, the dissertation is a yearlong activity, to be carried out and evaluated in two phases i.e. Phase – I: July to December and Phase – II: January toJune.
- The dissertation may be carried out preferably in-house i.e. department‟s laboratories and centers OR in industry allotted through department‟s T & Pcoordinator.
- After multiple interactions with guide and based on comprehensive literature survey, the student shall identify the domain and define dissertation objectives. The referred literature should preferably include IEEE/IET/IETE/Springer/Science Direct/ACM journals in the areas of Computing and Processing (Hardware and Software), Circuits-Devices and Systems, Communication-Networking and Security, Robotics and Control Systems, Signal Processing and Analysis and any other related domain. In case of Industry sponsored projects, the relevant application notes, while papers, product catalogues should be referred andreported.
- Student is expected to detail out specifications, methodology, resources required, critical issues involved in design and implementation and phase wise work distribution, and submit the proposal within a month from the date ofregistration.
- Phase – I deliverables: A document report comprising of summary of literature survey, detailed

objectives, project specifications, paper and/or computer aided design, proof of concept/functionality, part results, A record of continuousprogress.

- Phase – I evaluation: A committee comprising of guides of respective specialization shall assess the progress/performance of the student based on report, presentation and Q &A. In case of unsatisfactory performance, committee may recommend repeating the Phase-Iwork.
- During phase – II, student is expected to exert on design, development and testing of the proposed work as per the schedule. Accomplished results/contributions/innovations should be published in terms of research papers in reputed journals and reviewed focused conferences OR IP/Patents.
- Phase – II deliverables: A dissertation report as per the specified format, developed system in the form of hardware and/or software, a record of continuous progress.
- Phase – II evaluation: Guide along with appointed external examiner shall assess the progress/performance of the student based on report, presentation and Q &A. In case of unsatisfactory performance, committee may recommend for extension or repeating thework